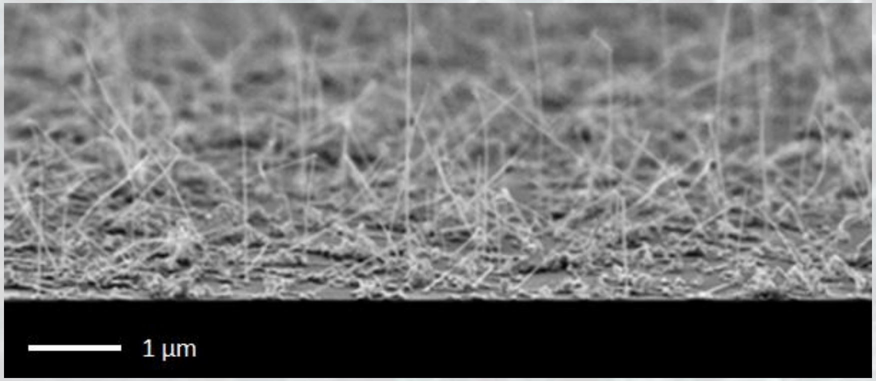
Nano Innovation 2016 Rome, 20-23 September

Conference & Exhibition

Chalcogenide nanowires for scaled phase change memories: opportunities and challenges



Massimo Longo

CNR-IMM

Agrate B.^{za} - Milan

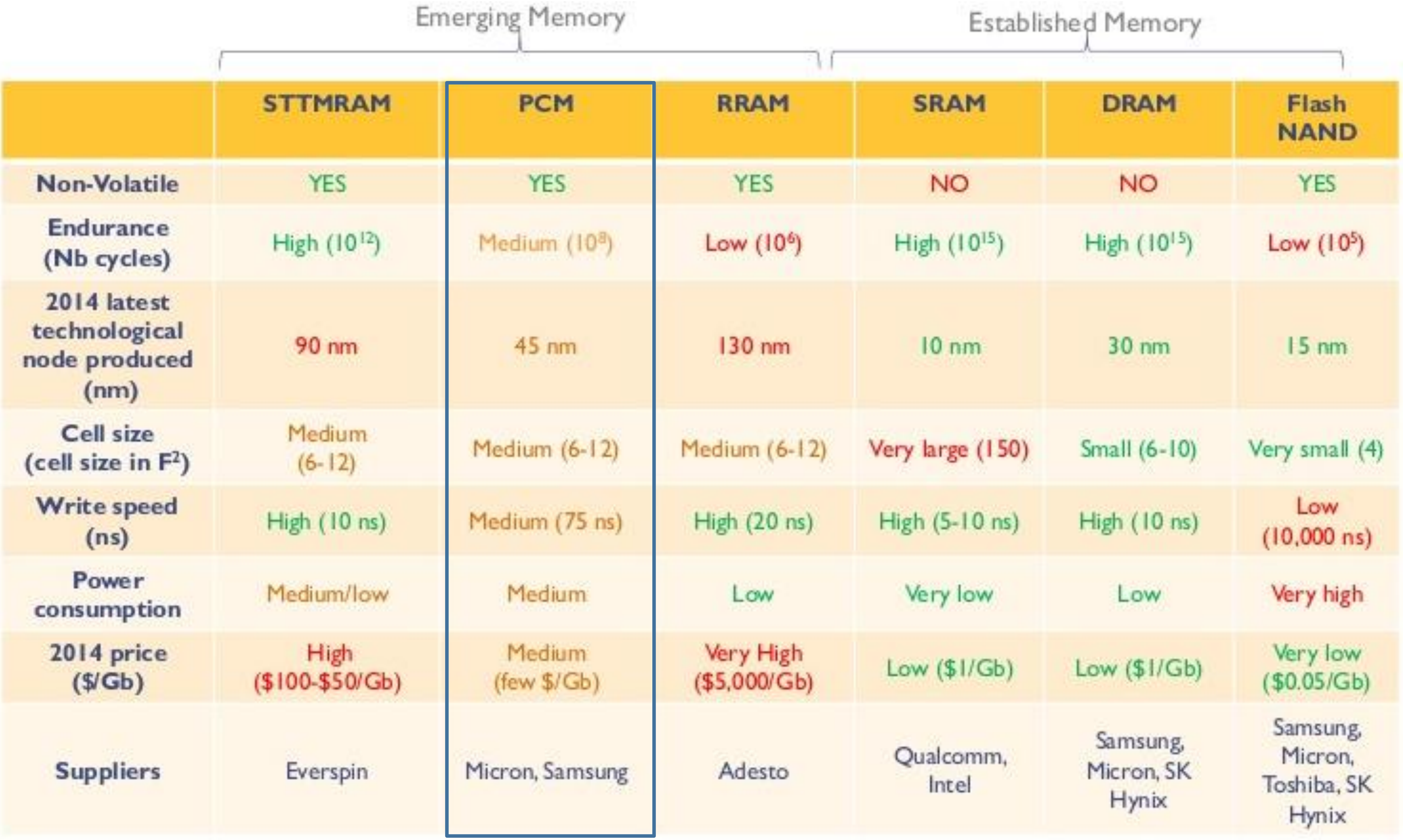
ITALY

IMM Institute for Microelectronics and Microsystems

Outline

- **Phase Change memory (PCM) cells**
- **Potentialities and issues of phase change nanowires (NWs)**
- **MOCVD self-assembly, modelling, functional analysis and positioning of Ge-Sb-Te, In-Sb-Te and In-Ge-Te NWs**
- **Conclusions**

Electronic memories



	Emerging Memory			Established Memory		
	STTMRAM	**PCM**	**RRAM**	**SRAM**	**DRAM**	**Flash NAND**
Non-Volatile	YES	YES	YES	NO	NO	YES
Endurance (Nb cycles)	High (10^{12})	Medium (10^{8})	Low (10^{6})	High (10^{15})	High (10^{15})	Low (10^{5})
2014 latest technological node produced (nm)	90 nm	45 nm	130 nm	10 nm	30 nm	15 nm
Cell size (cell size in F^2)	Medium (6-12)	Medium (6-12)	Medium (6-12)	Very large (150)	Small (6-10)	Very small (4)
Write speed (ns)	High (10 ns)	Medium (75 ns)	High (20 ns)	High (5-10 ns)	High (10 ns)	Low (10,000 ns)
Power consumption	Medium/low	Medium	Low	Very low	Low	Very high
2014 price ($/Gb)	High ($100-$50/Gb)	Medium (few $/Gb)	Very High ($5,000/Gb)	Low ($1/Gb)	Low ($1/Gb)	Very low ($0.05/Gb)
Suppliers	Everspin	Micron, Samsung	Adesto	Qualcomm, Intel	Samsung, Micron, SK Hynix	Samsung, Micron, Toshiba, SK Hynix

Phase Change Memory (PCM)

PCM-related last highlights

JULY 2015

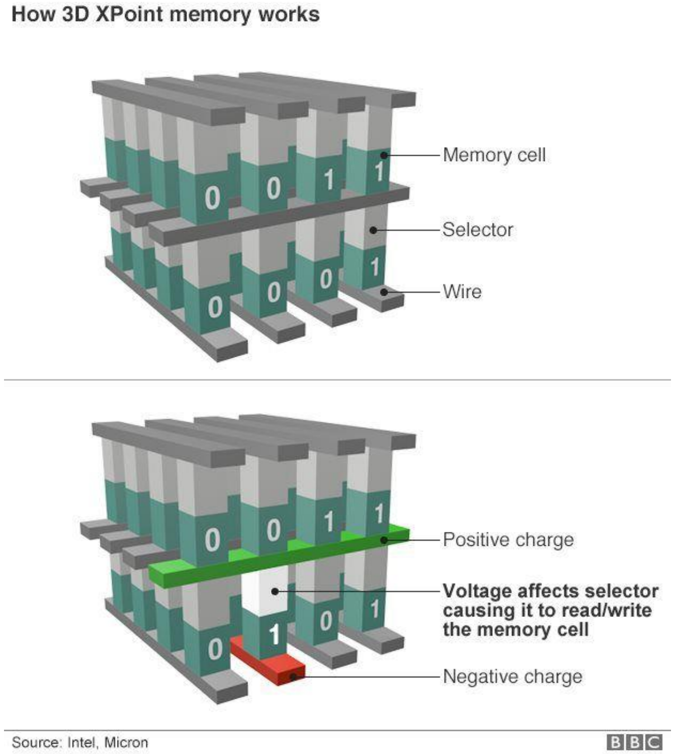
Intel and Micron: 3D Xpoint announced

Phase change alloy, (the most studied for PCM is Ge-Sb-Te), is used as a storage part of a memory cell.

Transistor-less, cells to be addressed individually.

High-density, high-speed memory.

https://www.micron.com/about/emerging-technologies/3d-xpoint-technology



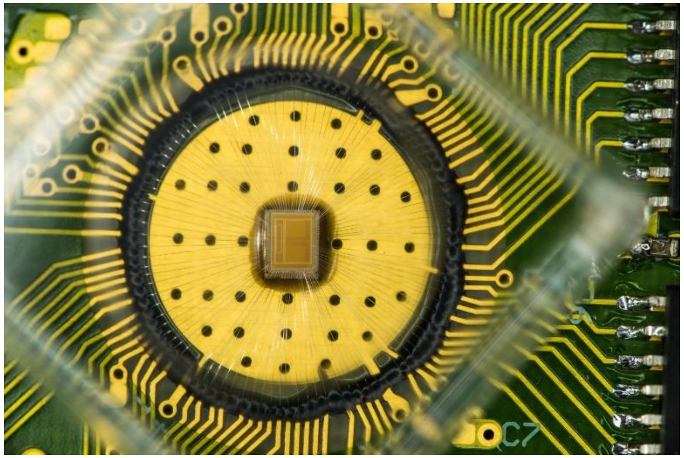
Source: Intel, Micron

May 2016

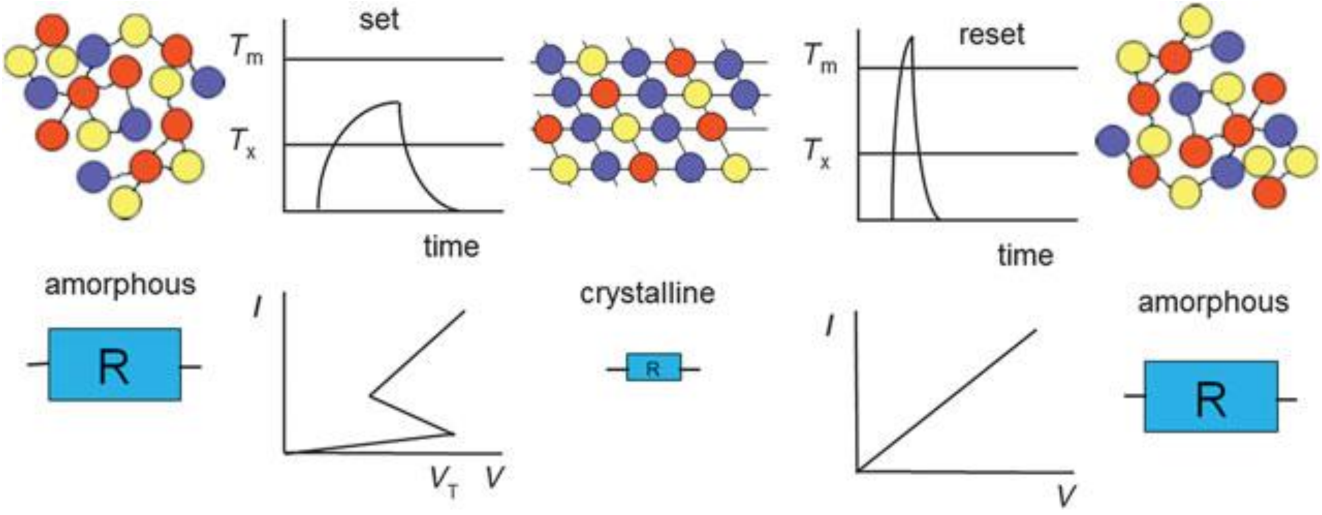
IBM demonstrated reliably storing 3 bits of data per cell

The memory array size is 2 × 1000 µm × 800 µm. The PCM cells are based on doped-chalcogenide alloy, integrated into the prototype chip serving as a characterization vehicle in 90 nm CMOS baseline technology.

http://m.phys.org/news/2016-05-ibm-scientists-storage-memory-breakthrough.html

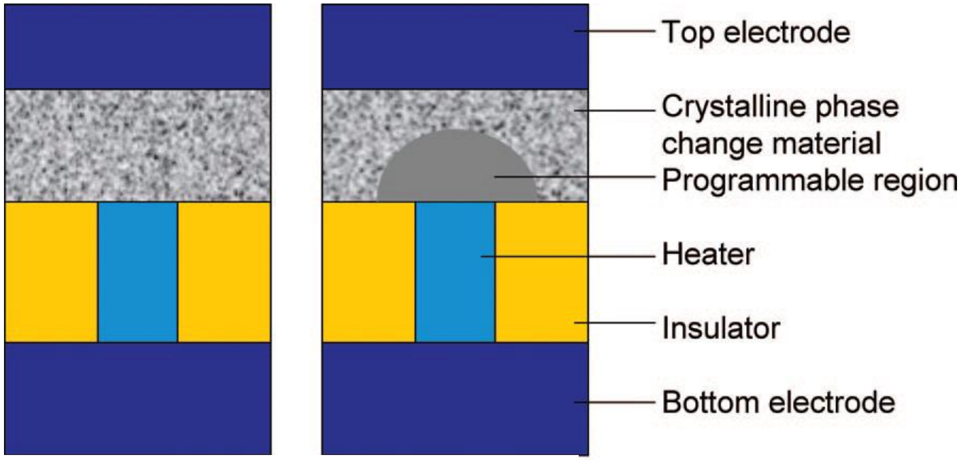


Principle of a Phase Change Memory (PCM)



BINARY DATA STORAGE:

RESET **SET**



amorphous
≈100 Ωcm

crystalline
≈1 mΩcm

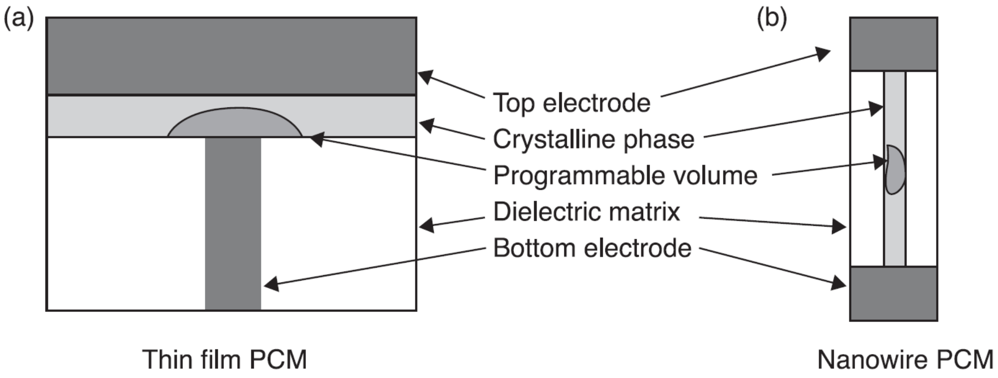
PCM Scaling for better performances:
reduction of I_{prog} and power consumption

Active material modification (composition, doping, resistivity), contact size, volume reduction, confined cells, interfacial effects, 3D cross-bar geometry.

Raoux et al., Chem. Rev. 110, 240–267 (2010) and MRS Bulletin 2014

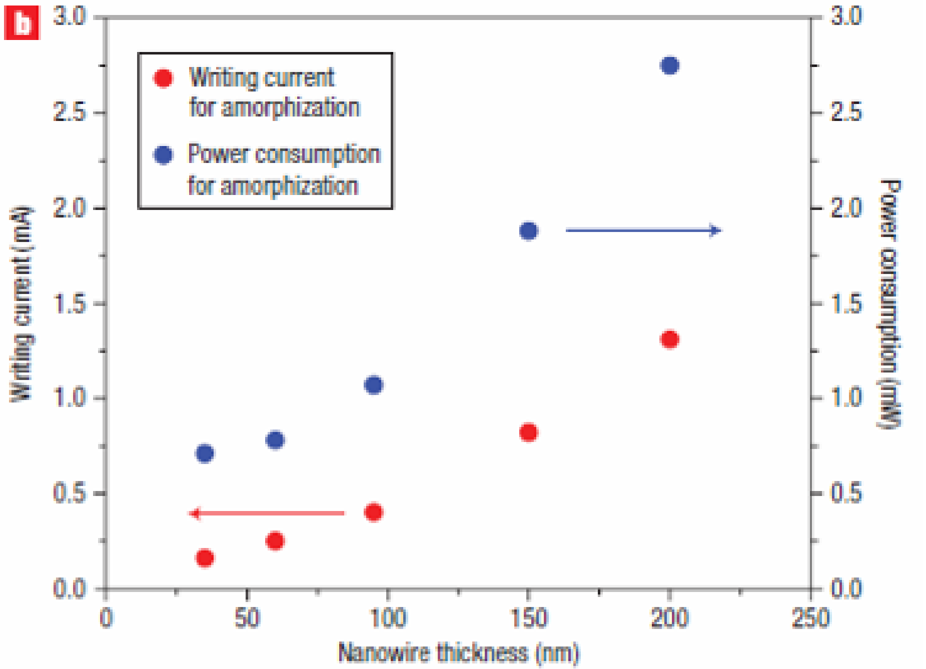
Promising performances of NW-based PCMs

M. Longo, Woodhead Publishing, 2014.



Strong reduction of active material volumes to be programmed → shorter and less intense current pulses.

- Self heating resistors
- Reduced chalcogenide/electrodes contact areas
- Low-cost manufacturing
- Self-assembly → defect-free NWs and core-shell geometry with a single step process

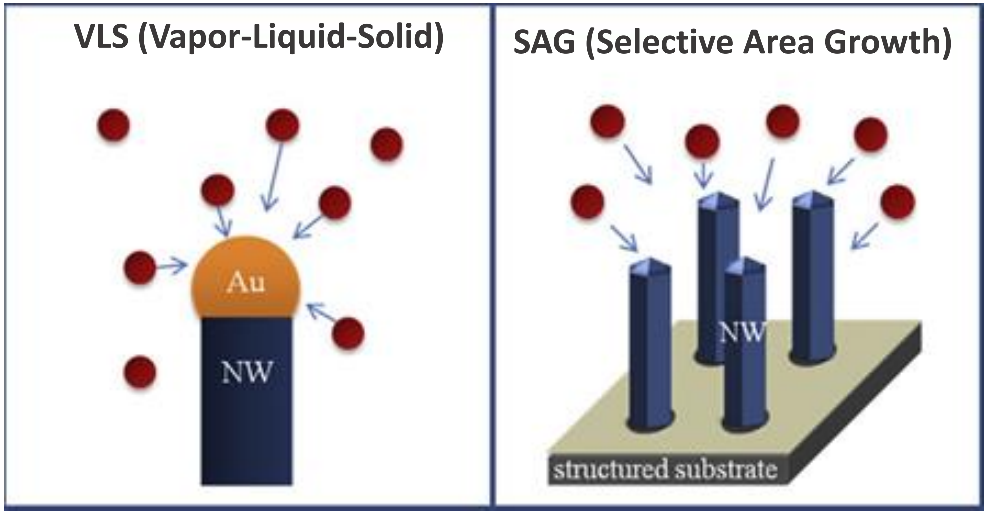


Competitive with top-dow approach!

Lee et al., Nat. Nanotechnology 2, 626 - 630 (2007)

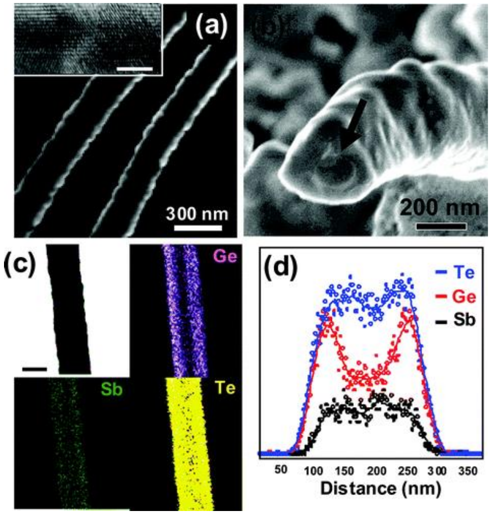
The NW self-assembly by Chemical Vapor Deposition

H. Hardtdegen et al., Progress in Crystal Growth and Characterization of Materials, 61 (2015) 27



Other catalyst-free methods (supersaturation driven protrusions)

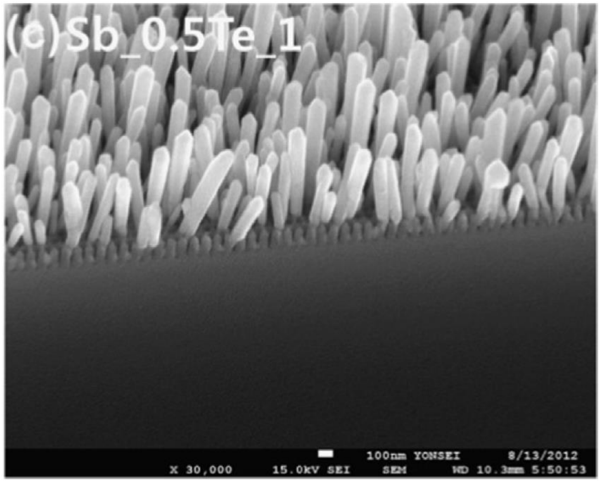
Phase change $GeTe/Ge_2Sb_2Te_5$ core-shell NWs by CVD



Jung et al, Nano Lett., 2008

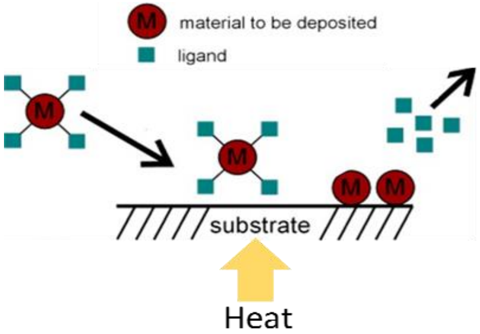
Challenge: Positioning and contacting of single NWs!

Te-rich SbTe NWs by AVD on trench-structured substrates



J.H. Jeongetal. et al., J. Cryst. Growth, 410 (2015) 47

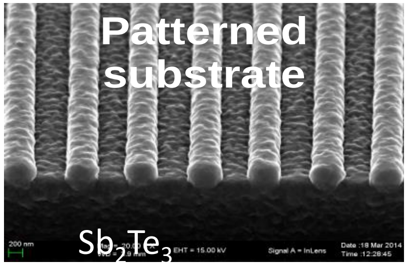
MOCVD growth at CNR-IMM, unit of Agrate



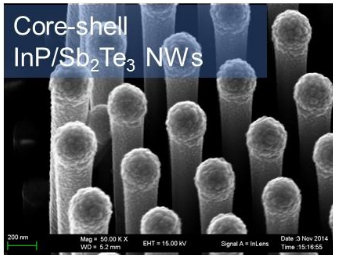
4” MOCVD reactor for films and nanostructures

- Precursors for In, Ge, Te, Sb
- Growth time: 60 - 210 min
- Growth temperature: 400 - 450°C,
- Pressure: 400-500 mbar.

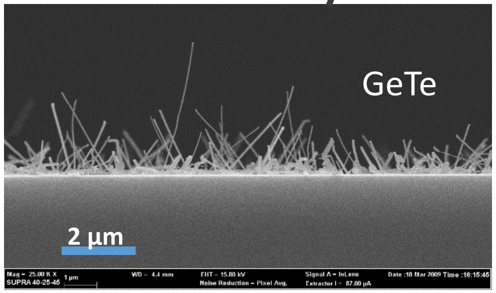
Conformal films

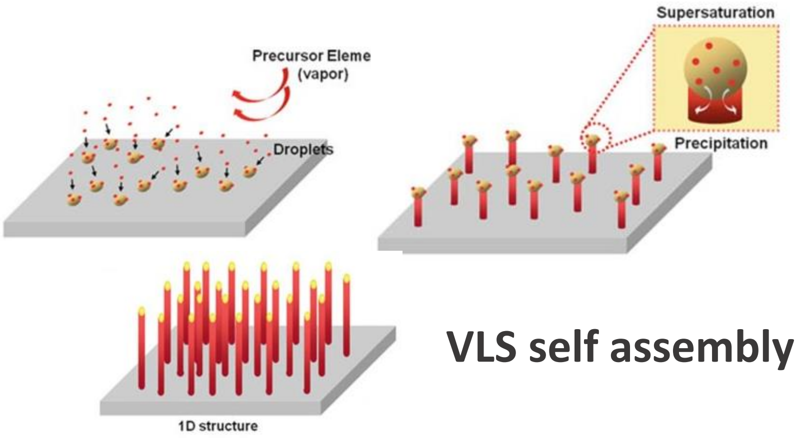


Conformal 3D overgrowth



Nanowires by VLS

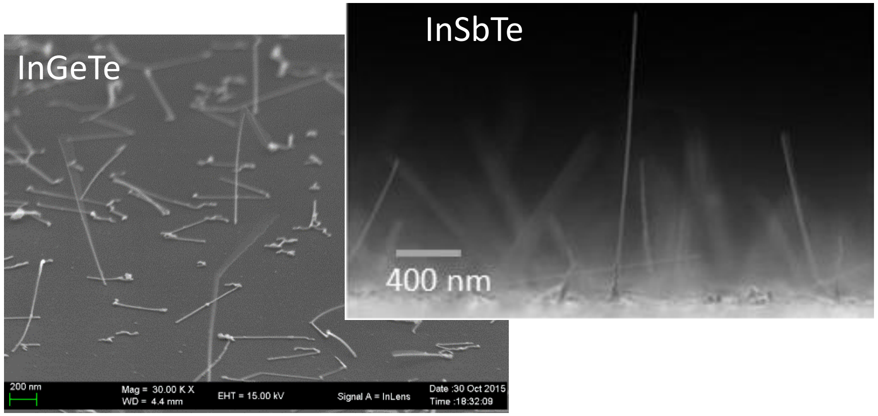




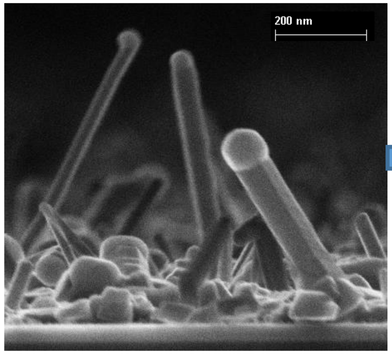
VLS self assembly

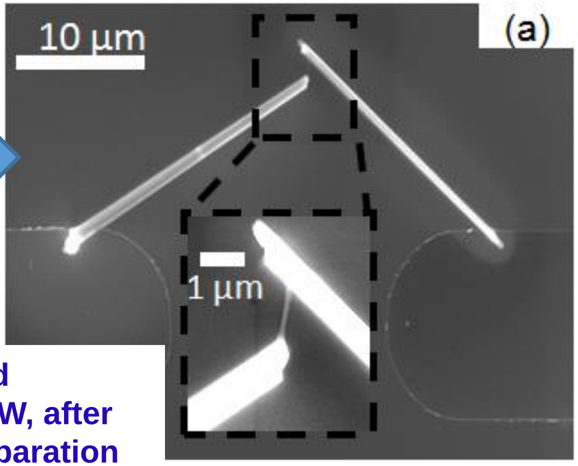
- Si(100), Si(111), Si(110) or patterned substrates
- Au NPs sizes: 10, 15, 20, 30 and 50 nm

In-based chalcogenide have much higher thermal stability → higher data retention

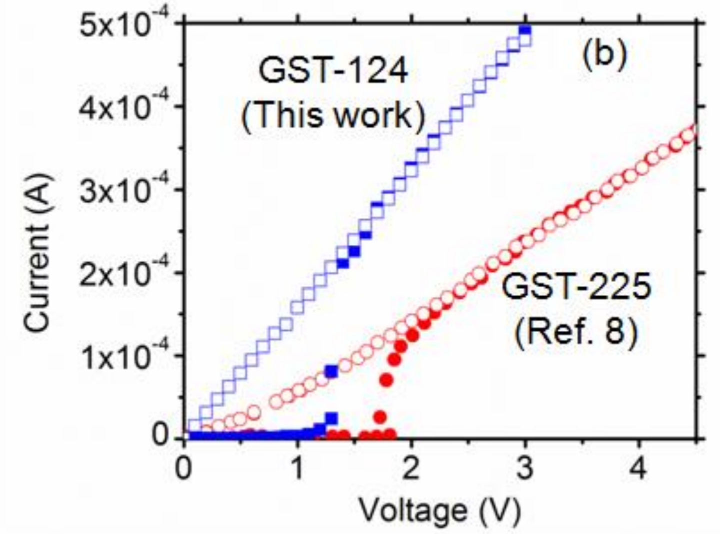


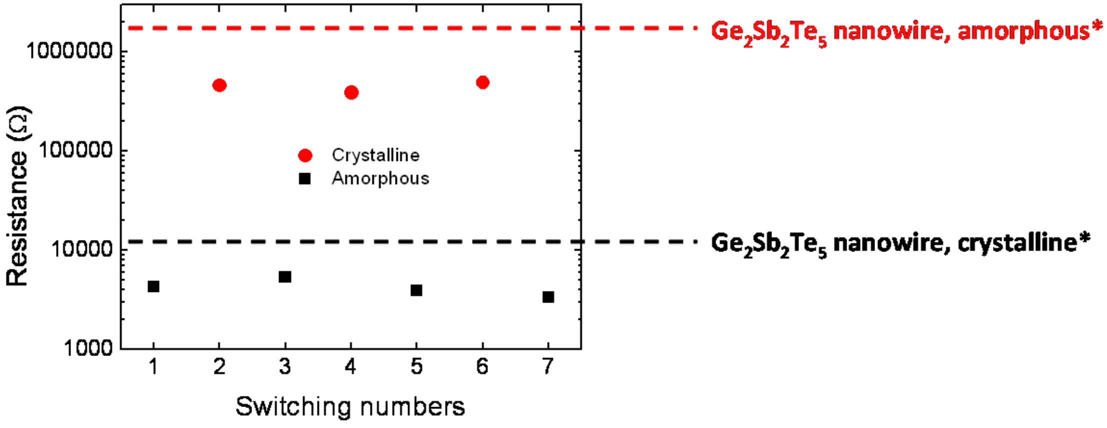
Phase change in a $Ge_1Sb_2Te_4$ NW by MOCVD-VLS





1 µm long and 80 nm wide NW, after electrode preparation





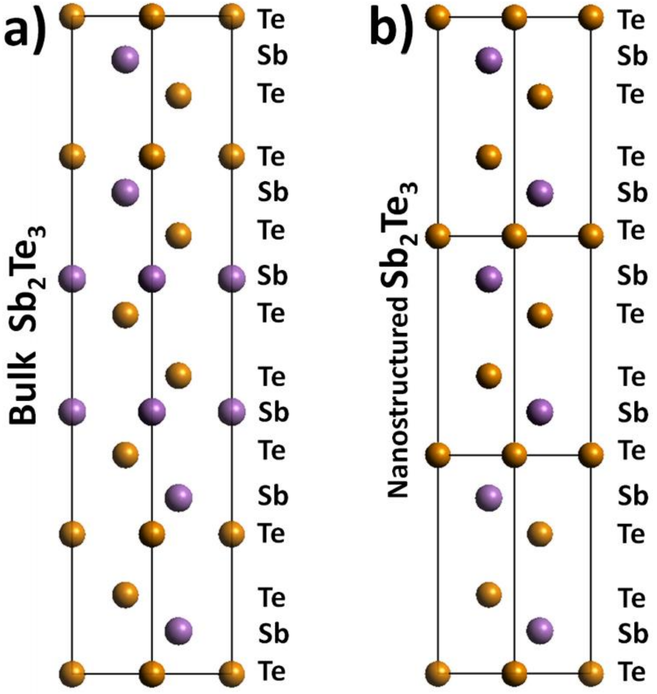
[pulses: am.: 3 V, 300 ns cr.: 1 V, 500 ns]

M. Longo et al.,
Nano Lett., 12 (2012) 1509

*by evaporation of GeTe and Sb_2Te_3 powders, 60 nm Ø
[Lee et al., Nature Nanotechnology 2, 626 - 630 (2007)]

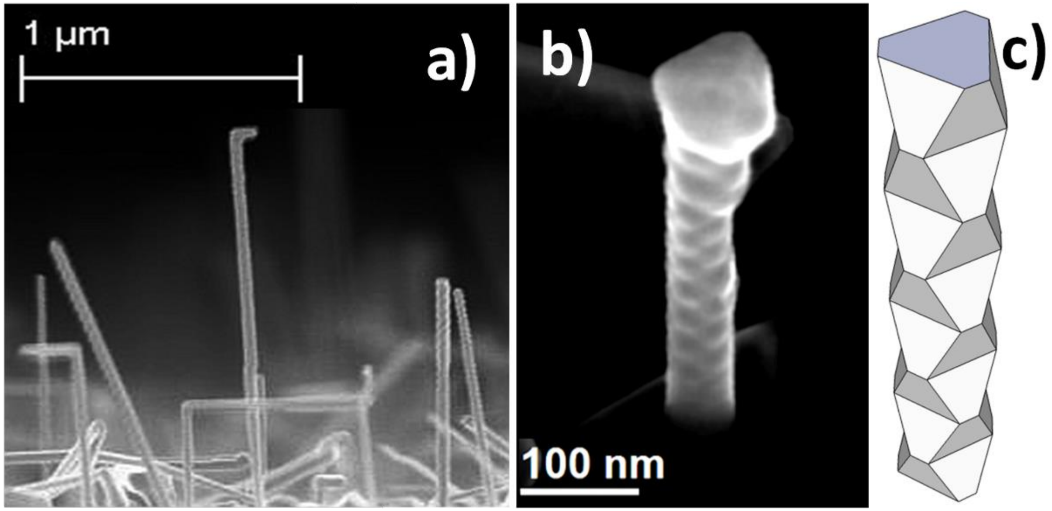
Lower threshold voltage (1.35 eV), smaller programming window than in $Ge_2Sb_2Te_5$ NWs and lower threshold voltage than in thin film devices based on $Ge_1Sb_2Te_4$ (1.41 eV, JJAP, 45 (2006) 3955).

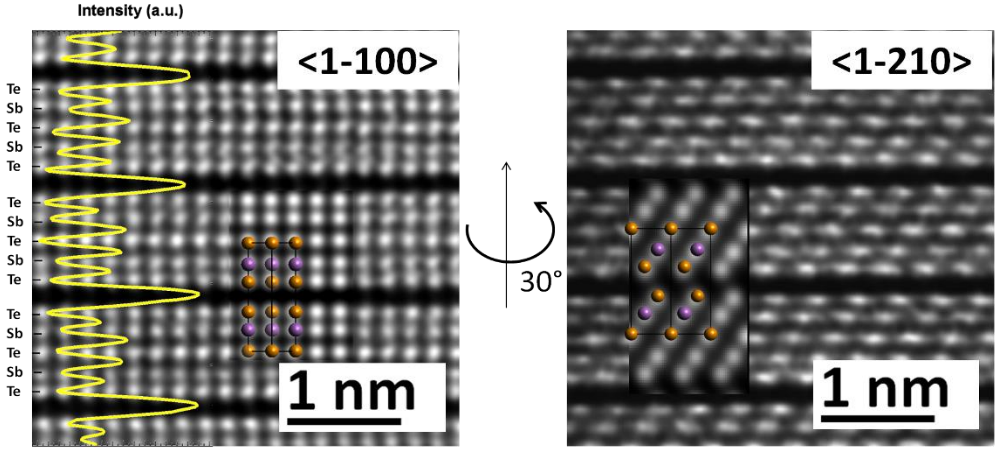
A novel Sb_2Te_3 polymorph by MOCVD-VLS



SG #166 **SG #164**

The polymorph crystallizes in the SG# 164 trigonal phase and is stable at the nanoscale, due to the particular side-wall nanofaceting, as confirmed by first principle calculations.





E. Rotunno et al. Chem. Mater., 2015, 27 4368

Crystallization kinetics by MD simulations

How does nanostructuring affect the crystallization speed?

Simulated crystallization kinetics in a phase change GeTe nanowire

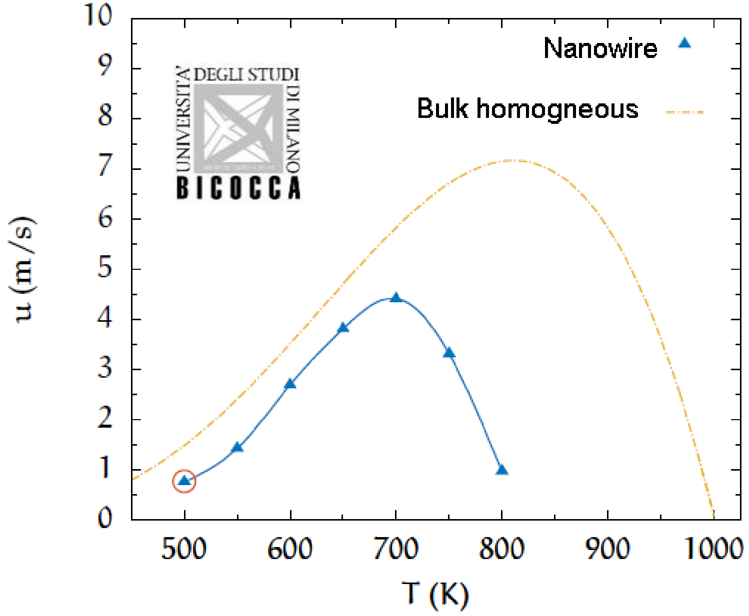
after amorphization

Diam.
8 nm
16500
atoms

after recrystallization

The thermal conductivity of a fully crystalline GeTe NW computed in a 30000-atom model turns out to be about one half lower than the corresponding bulk value

Maximum crystal growth velocity

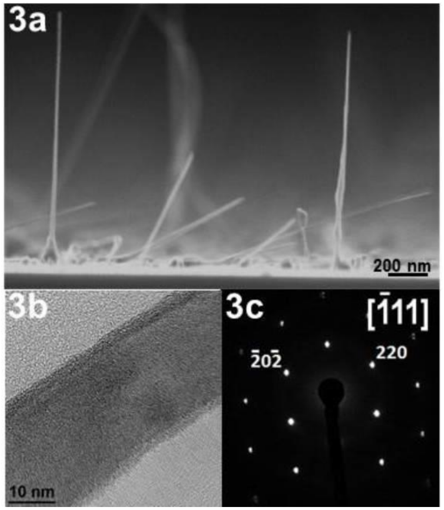


Lowering of melting from 1000 K in the bulk to about 830 K in the NW

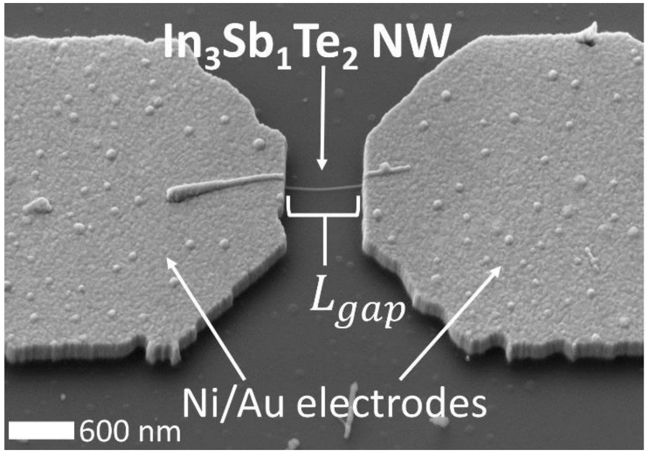
E. Bosoni et al., NVM Workshop, 2016

Phase change of In-Sb-Te NWs

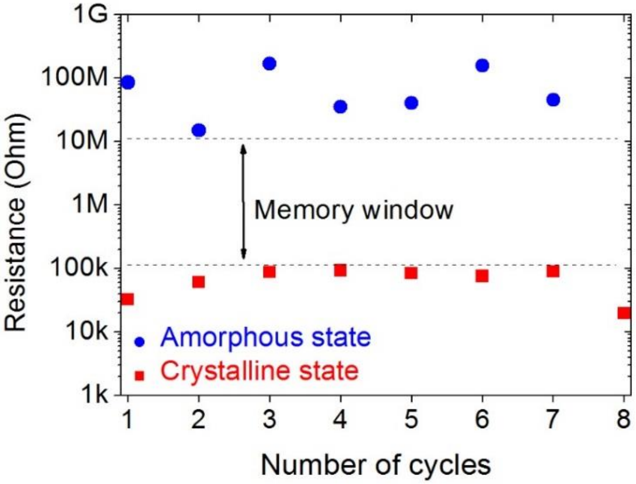
Single crystals $In_3Sb_1Te_2$ NWs by VLS

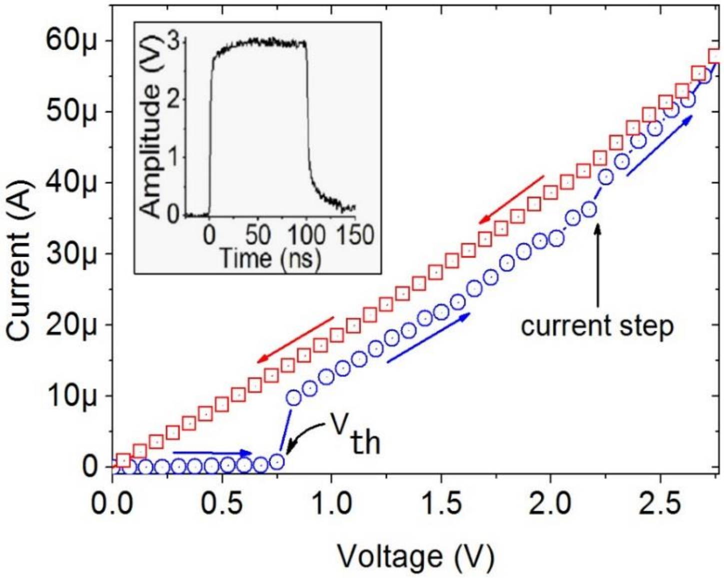


S. Selmo et al. PSSA 2016

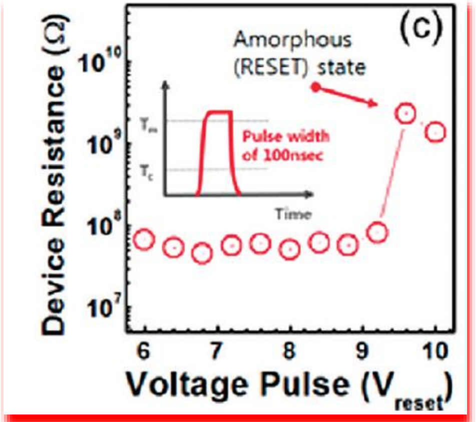


Reversible non volatile PCM switch





- 10 switching cycles
- Power consumption = 10^{-4} W → 1/5 of 30 nm wide GST NWs (Lee, Nanotechnology 2007)
- Reset pulse = 1/3 of 60 nm wide IST NWs

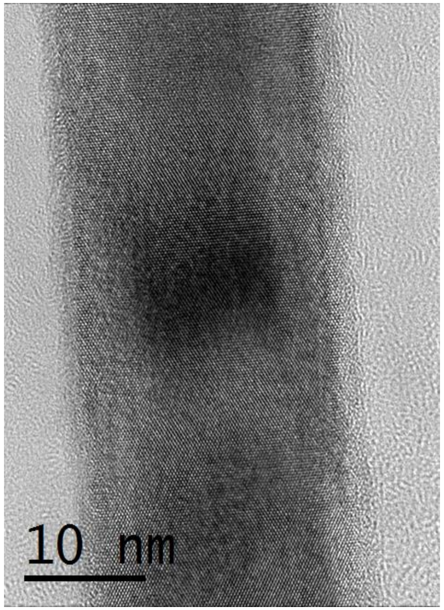


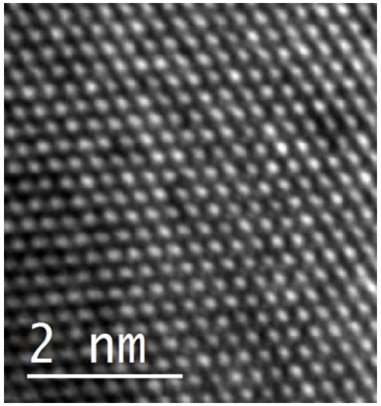
Ahn, Nanolett., 2010

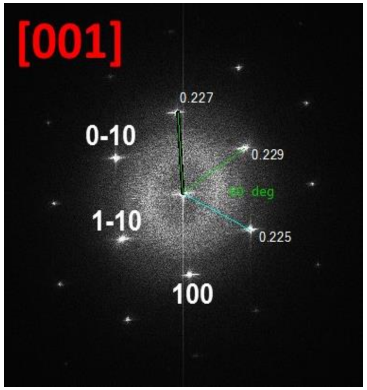
S. Selmo et al., submitted

In-doped Sb NWs

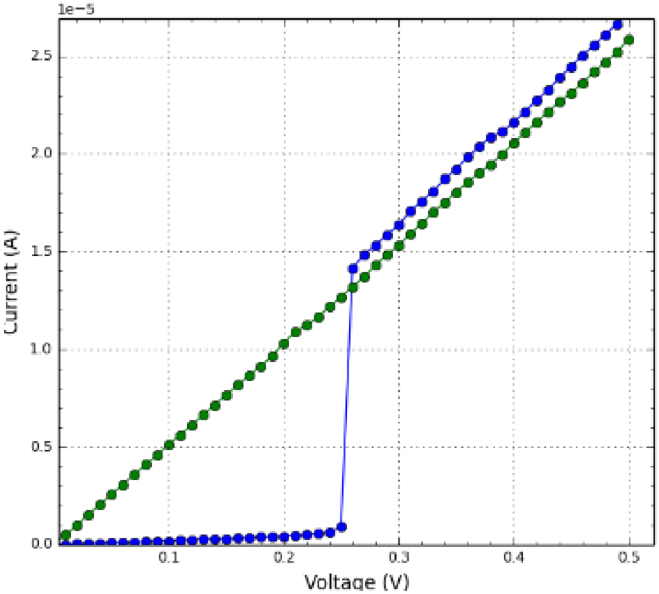
Single crystal In-Sb NWs by VLS







Reversible and very fast (25 ns pulse for re-crystallization) non volatile PCM switch

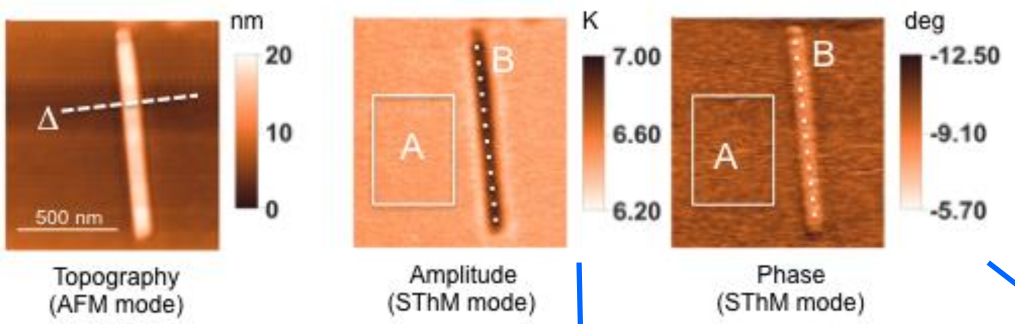


S. Selmo, Unpublished

Thermal resistance R_{NW} of $In_3Sb_1Te_2$ NWs by SThM-3 Ω

$$R_{NW} = e_{NW} / k_{NW}$$

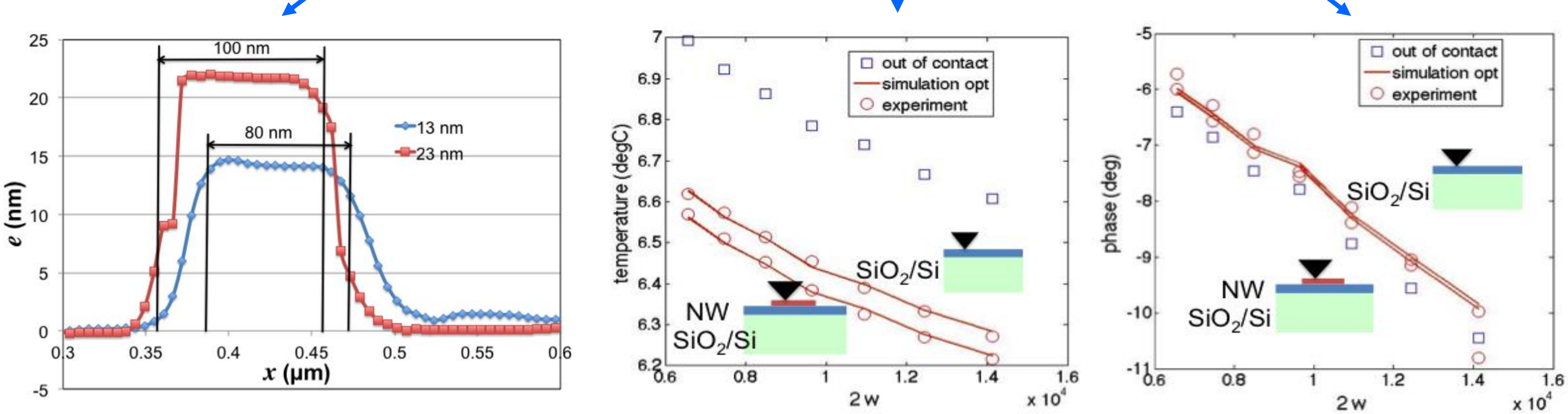
e_{NW} = thickness



Topography (AFM mode)

Amplitude (SThM mode)

Phase (SThM mode)



Bulk phonon mfp = 3 $K_{bulk}/\rho v_{sound} C_p$ = 20.7 nm

Thermal cond. K_{bulk} = 21 W·m/K →

$R_{NW,\ 23nm\ bulk}$ = 1.09×10^{-9} K·m²/W

$R_{NW,\ 13nm\ bulk}$ = 6.19×10^{-10} K·m²/W

$R_{NW,\ 23nm}$ = $(9.45 \pm 1.41) \times 10^{-9}$ K·m²/W

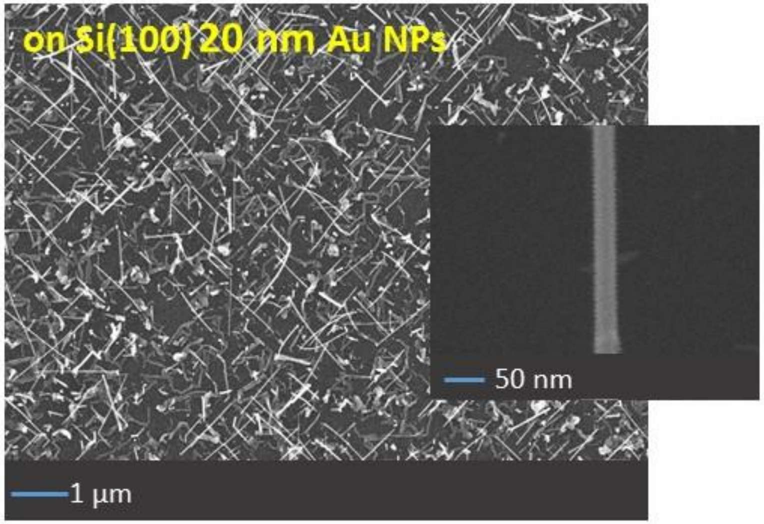
$R_{NW,\ 13nm}$ = $(6.45 \pm 0.97) \times 10^{-9}$ K·m²/W

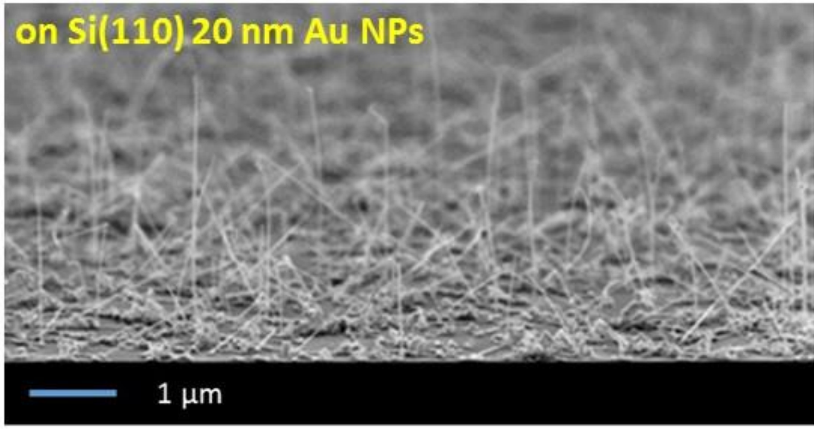
Higher than calculated from K_{bulk} → Phonon confinement!

J.-L. Battaglia et al., submitted

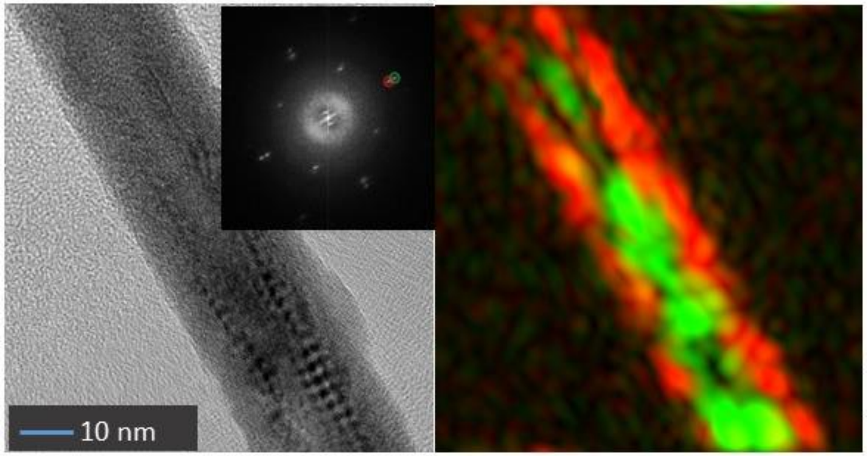
In-Ge-Te NWs

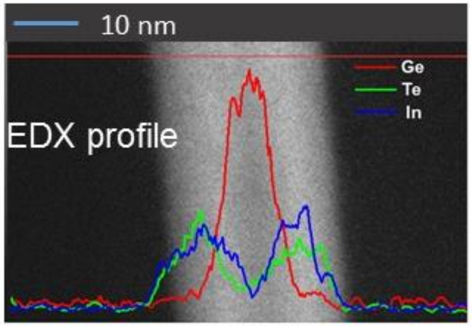
SEM





TEM





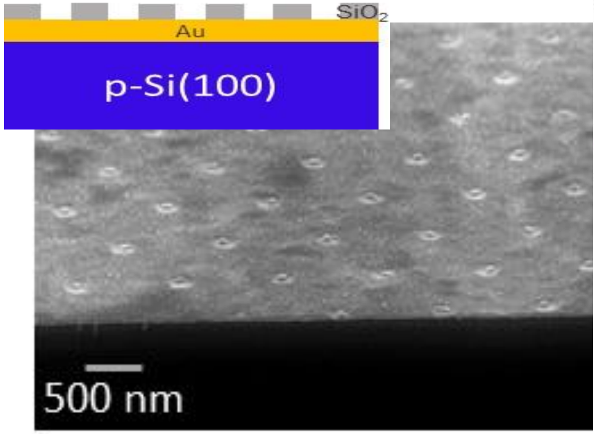
Core-shell NWs

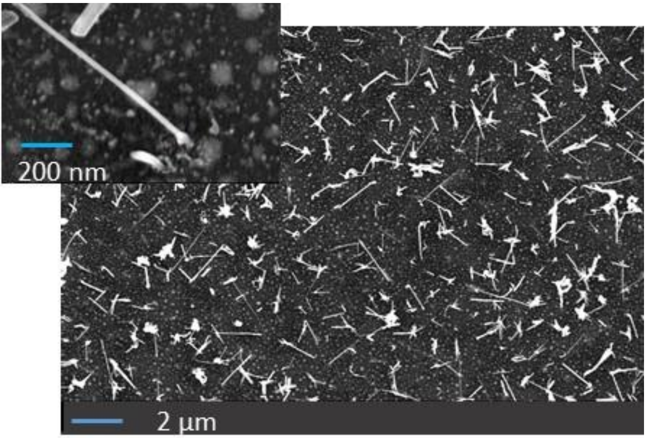
- Core lattice compatible with d_{220} of cubic Ge
- Shell compatible with d_{220} of cubic InTe
- Core and shell lattices in epitaxial relationship

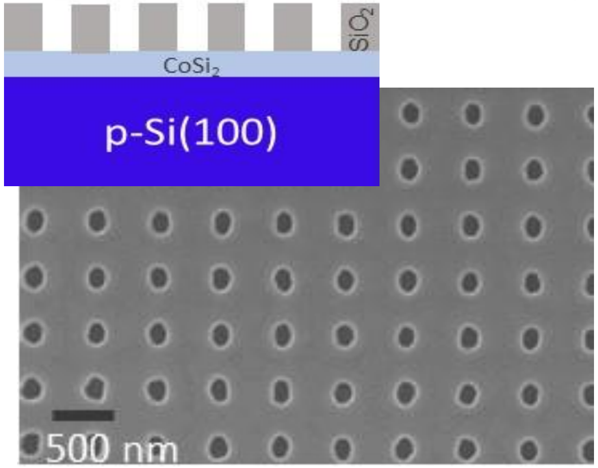
R. Cecchini et al. , in preparation

In-Ge-Te NWs arrays

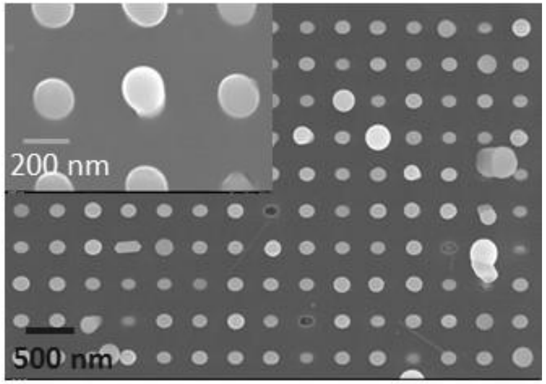
Unpublished



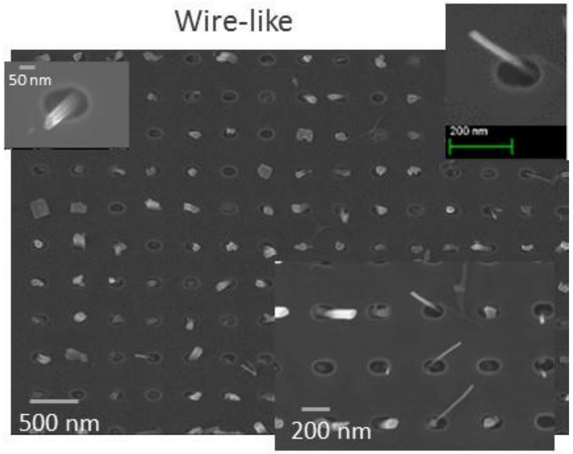


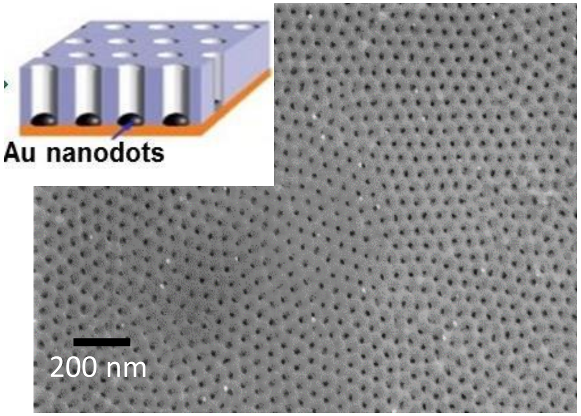


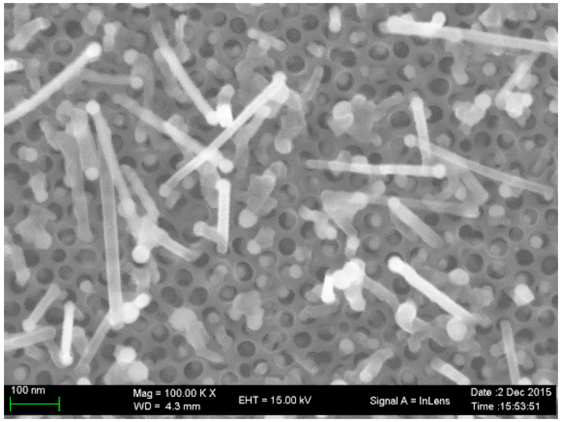
“Mushroom”-like

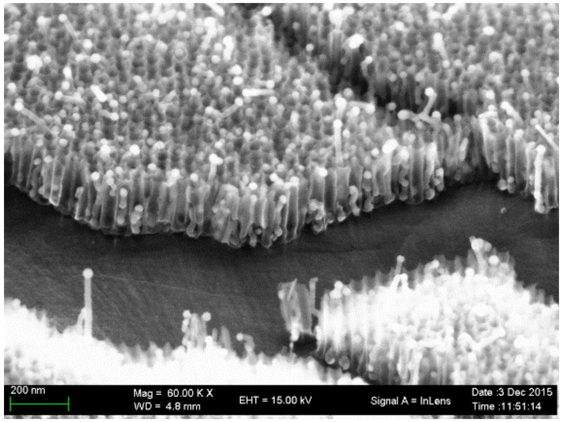


Wire-like





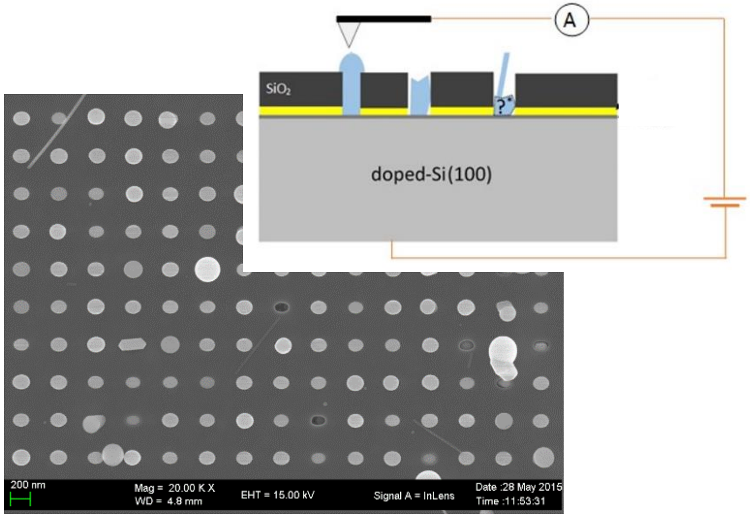




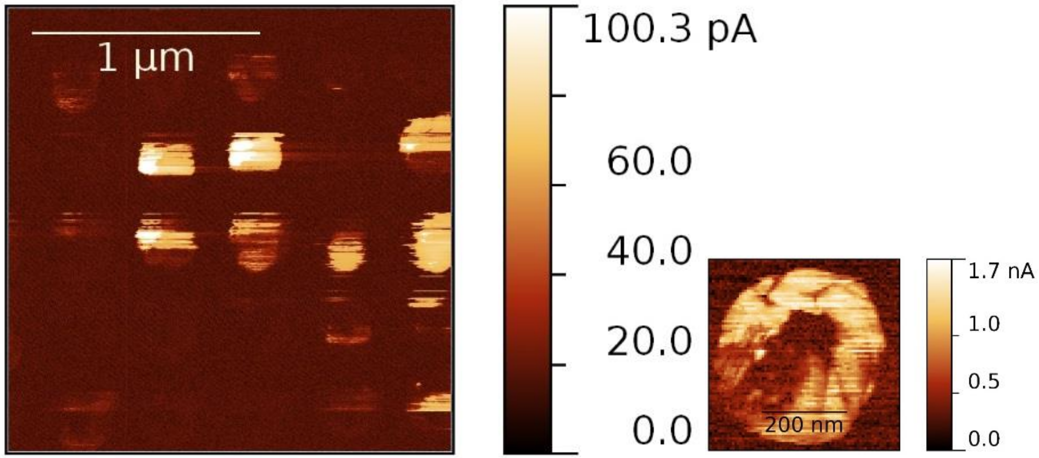
IGT Nanopillar-based cells characterization

Agrate Brianza

Tyndall National Institute



SEM of In-Ge-Te nano-pillars array



C-AFM of In-Ge-Te nano-pillars array (left) and of single pillar (right)

Assessment of electrical testability of In-Ge-Te cells array on $CoSi_2$ contacted nanoholes.

Unpublished

Conclusions

- MOCVD processes for Ge-Sb-Te, In-Sb-Te, In-Ge-Te NWs growth on planar substrates were found (notable results: novel polymorph Sb-Te, low-power switching IST NWs, first and epitaxial IGT NWs).
- Simulations of crystallization kinetics in phase change nanowires
- Electrothermal analysis of NWs
- NWs growth on different patterned substrates were evaluated. IGT NWs and nano-pillars were obtained on metal-coated templates.

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Future work

- Complete assessment of electro-thermal properties for In-based NWs.
- Ordered array of NWs and electrical test.
- Synthesis of core-shell NWs for multilevel PCM.

Contributors and acknowledgements

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Vincenzo Grillo
Lucia Nasi

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TU-Vienna-Austria
Alois Lugstein

FZJ-Germany
Hilde Hardtdegen
Martin Schuck
Konrad Wirtz
Sally Riess
Kristof Keller
Gregor Mussler
Martin Mikulics

Tyndall Inst. Univ. Cork-Ireland
Paul Hurley
Scott Monagan
Karim Kerchaoui
Brendan Sheehan

CNRS-France
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Yannick Anguy
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G. C. Sosso
S. Gabardi

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SPARES

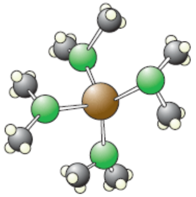
MOCVD at CNR: self assembled (Ge)Sb-Te NWs

Precursors

Ge Precursor

(TETRAKISDIMETHYLAMINO GERMANIUM)

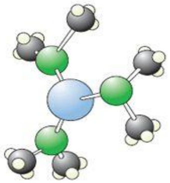
$Ge[N(CH_3)_2]_4$



Sb Precursor

(TRISDIMETHYLAMINOANTIMONY)

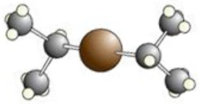
$[N(CH_3)_2]_3Sb$



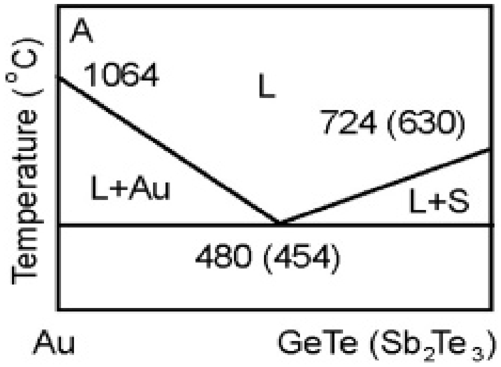
Te Precursor

(DIISOPROPYLTELLURIDE)

$(C_3H_7)_2Te$



Nano Lett., 6 (2006) 1514



Ge:Sb-Te

- High speed
- Low power PCM devices
- Topological insulator
- Thermoelectric material

Process parameters:

Substrates: SiO_2 and Si(001)

Au NPs sizes for VLS: 10-50 nm

Deposition time 20-90 min.

Temperature: 300 to 450°C

Reactor pressure: 50 to 450 mbar.

MOCVD - self assembly of In-Sb-Te NWs

$In_3Sb_1Te_2$ (IST)

Very high cryst, temp. (~290° C) → automotive applications

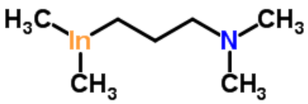
Multi-bit data storage: segregation of In-Sb/In-Te between 290 and 420° C

Precursors

In Precursor

Dimethylaminopropyl-dimethyl-indium

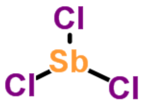
$C_7H_{18}InN$, DADI



Sb Precursor

Antimony tricloride

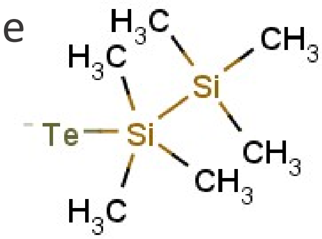
$SbCl_3$



Te Precursor

Bis(trimethylsilyl) telluride

$Te(SiMe_3)_2$, DSMTe



Process parameters:

Si(100), Si(110) substrates

Au NPs sizes for VLS: 10-50 nm

Deposition time 60-90 min.

Temperature: 300 to 425°C

Reactor pressure: 300 to 750 mbar.

MOCVD - self assembly of In-Ge-Te NWs

In-Ge-Te

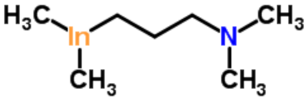
- Very high crystallization temperature (276°C)
- Very good retention of 10 years at 170°C

Precursors

In Precursor

Dimethylaminopropyl-dimethyl-indium

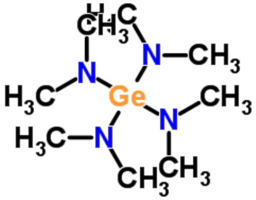
$C_7H_{18}InN$, DADI



Ge Precursor

Tetrakis(DiMethylAmino)Germanium

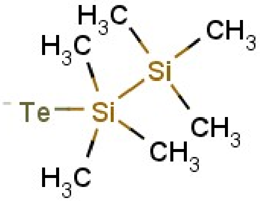
$Ge[N(CH_3)_2]_4$



Te Precursor

Bis(trimethylsilyl) telluride

$Te(SiMe_3)_2$, DSMTe



Process parameters:

Si(100), Si(111), Si(110) substrates

Au NPs sizes for VLS: 10, 20, 30 and 50 nm

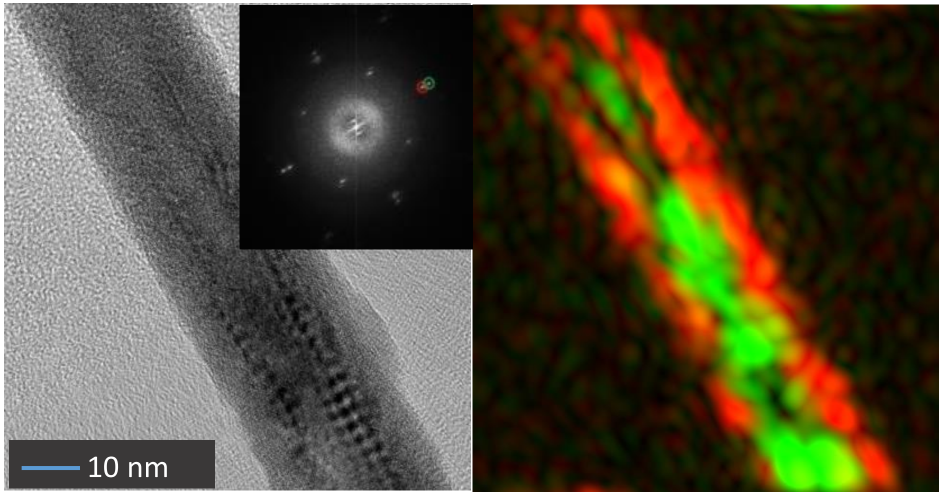
Deposition time 60-210 min.

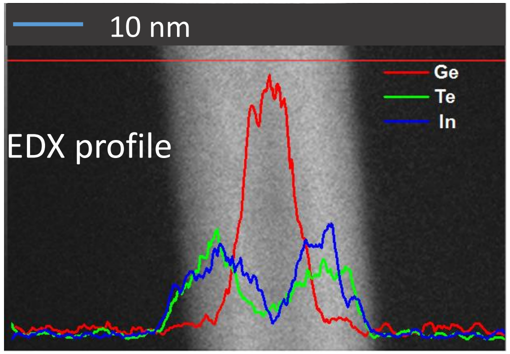
Temperature: 400 to 450°C

Reactor pressure: 400 to 500 mbar.

Microstructure: TEM + EDX

10 nm Au NPs

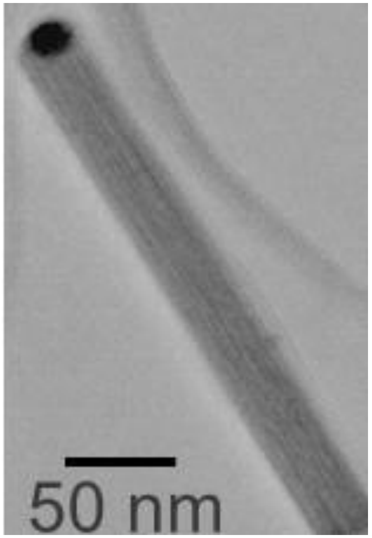




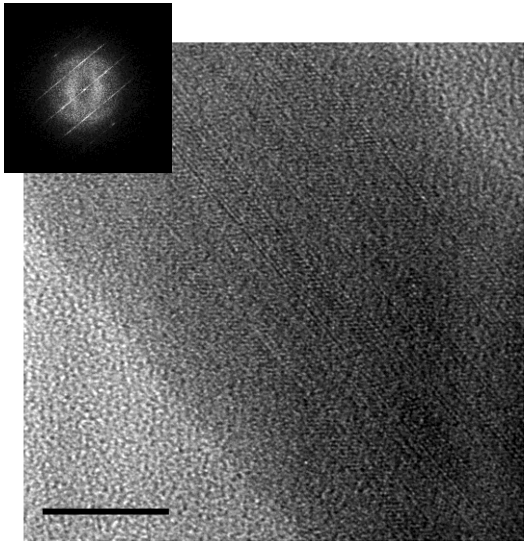
Core-shell NWs

- Core lattice compatible with d_{220} of cubic Ge
- Shell compatible with d_{220} of cubic InTe
- Core and shell lattices in epitaxial relationship

20 nm Au NPs



EDX: In_{33} Ge_{33} Te_{33} at %



EDX: In_{42} Ge_{10} Te_{48} at %

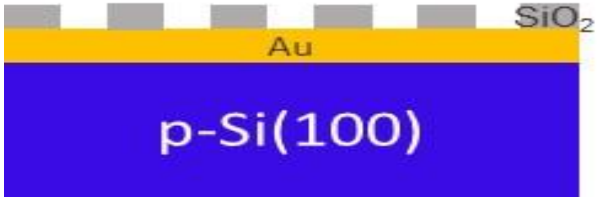
Ternary In-Ge-Te NWs

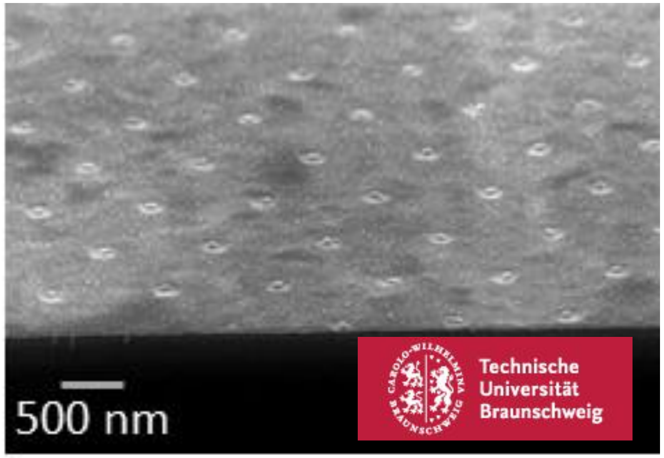
- Different compositions (EDX)
- Highly disordered

R. Cecchini et al., in preparation

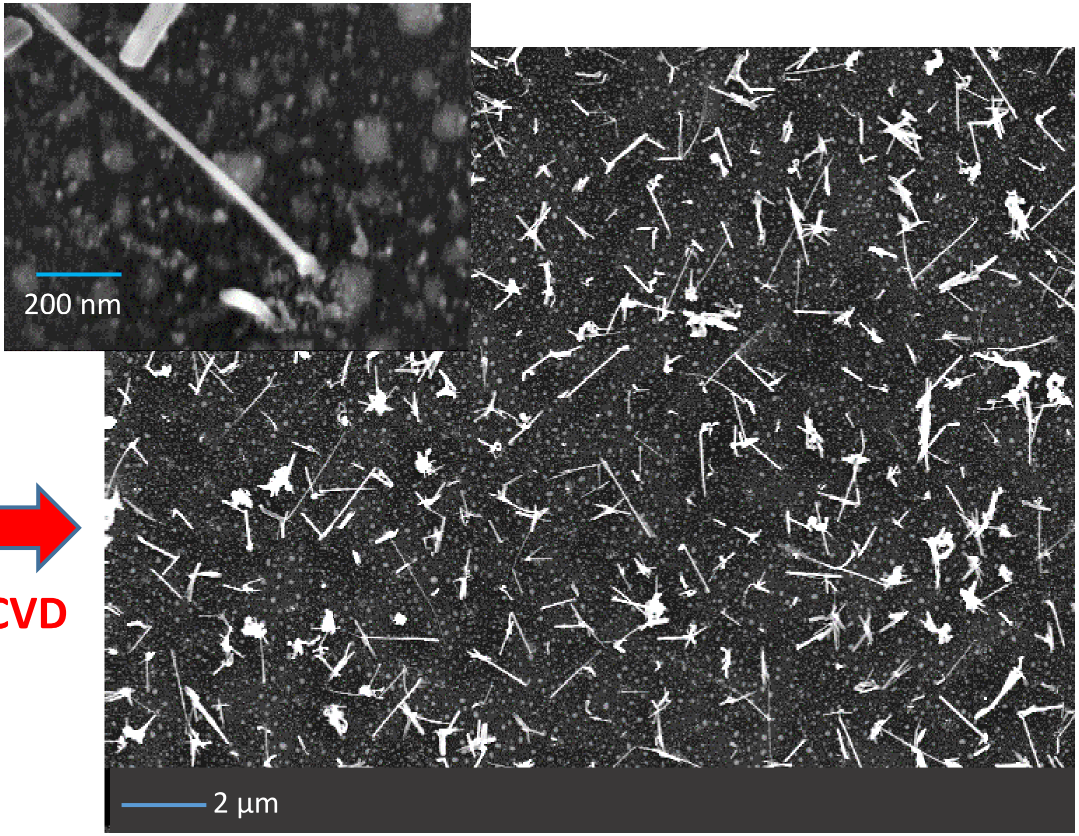
In-Ge-Te arrays positioning

Patterned substrate for VLS mechanism with Au film



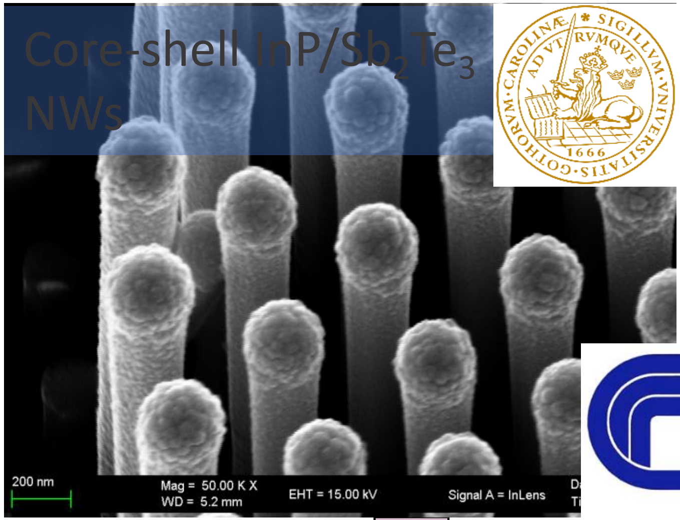


MOCVD



- Selective growth
- In some cases more than 1 NW/hole

Core-shell InP/Sb_2Te_3 NWs

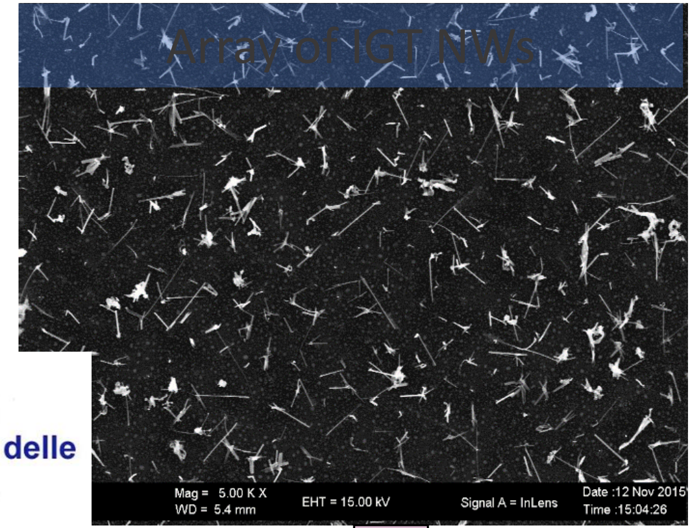


Conformal growth for In- and Ge-based chalcogenides

Multi level phase change

Consiglio Nazionale delle Ricerche

Array of IGT NWs



Use Si(110) substrate → vertical NWs

Reduce hole size →1 NW/hole

Use HSQ for embedment

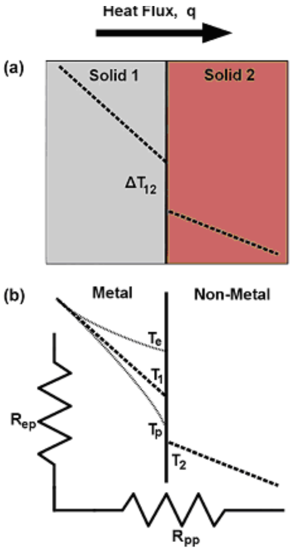
Best of WP3 - Simulations

Crystallization in NW, lower speed because of lower melting T, but still sufficiently high for PCM.

Microscopic origin of the resistance drift in amorphous phase of GeTe/GST (removal of Ge-Ge bonds).

Drift lower in NW because of fewer Ge-Ge bonds.

Gabardi et al, PRB 2015



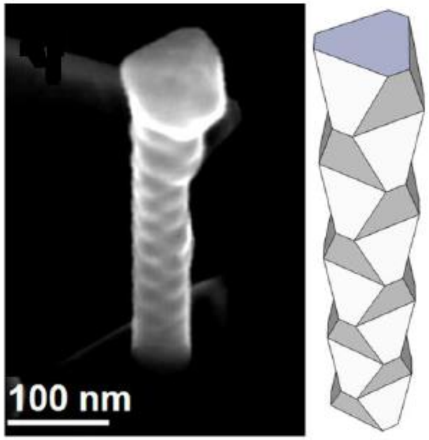
Uncovering of a strong electron-phonon contribution to the thermal boundary resistance for GeTe/GST (unusual). Important for electrothermal modeling of devices.

Campi et al, JAP 2015; JPCM 2015

Microscopic origin of peculiar shape of Sb_2Te_3 NWs grown at CNR.

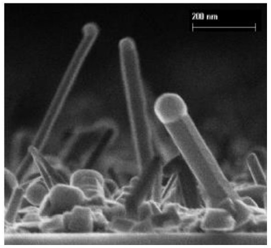
Rotunno et al. Chem. Mater. 2015

UNIVERSITA' DEGLI STUDI DI MILANO BICOCCA

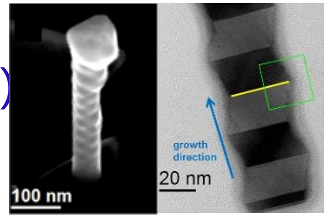


Best of WP4 – Deposition

GST NWs



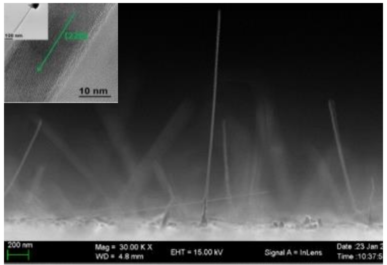
ST NWs
(new polymorph!)



E. Rotunno et al. Chem. Mater. (2015)

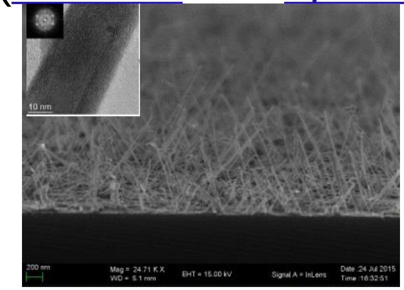
NWs growth
on flat substrates

IST NWs
(< 20 nm)



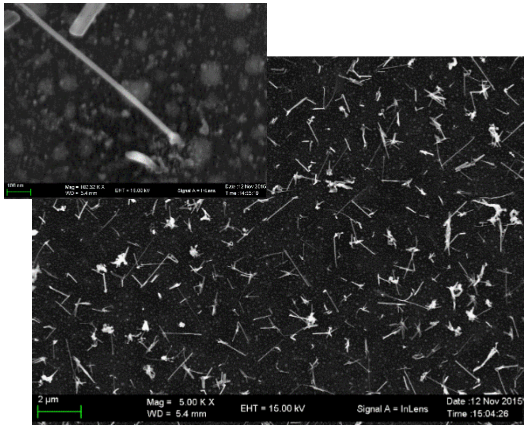
S. Selmo et al.
Phys. Status Solidi A (2015)

IGT NWs
(first time and epitaxy!)

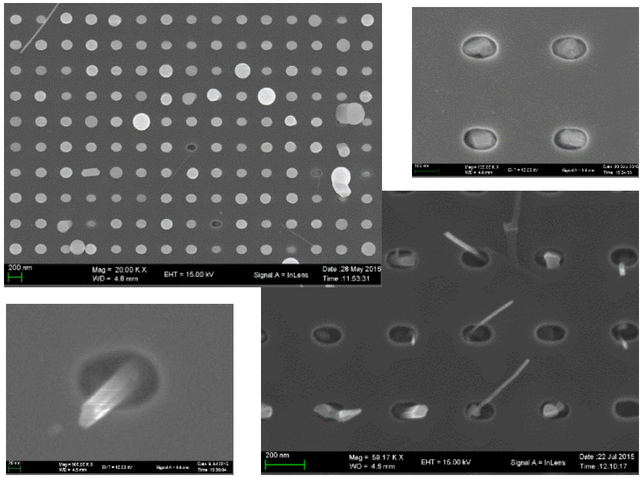


Consiglio
Nazionale delle
Ricerche

NWs and
nano-pillars
arrays

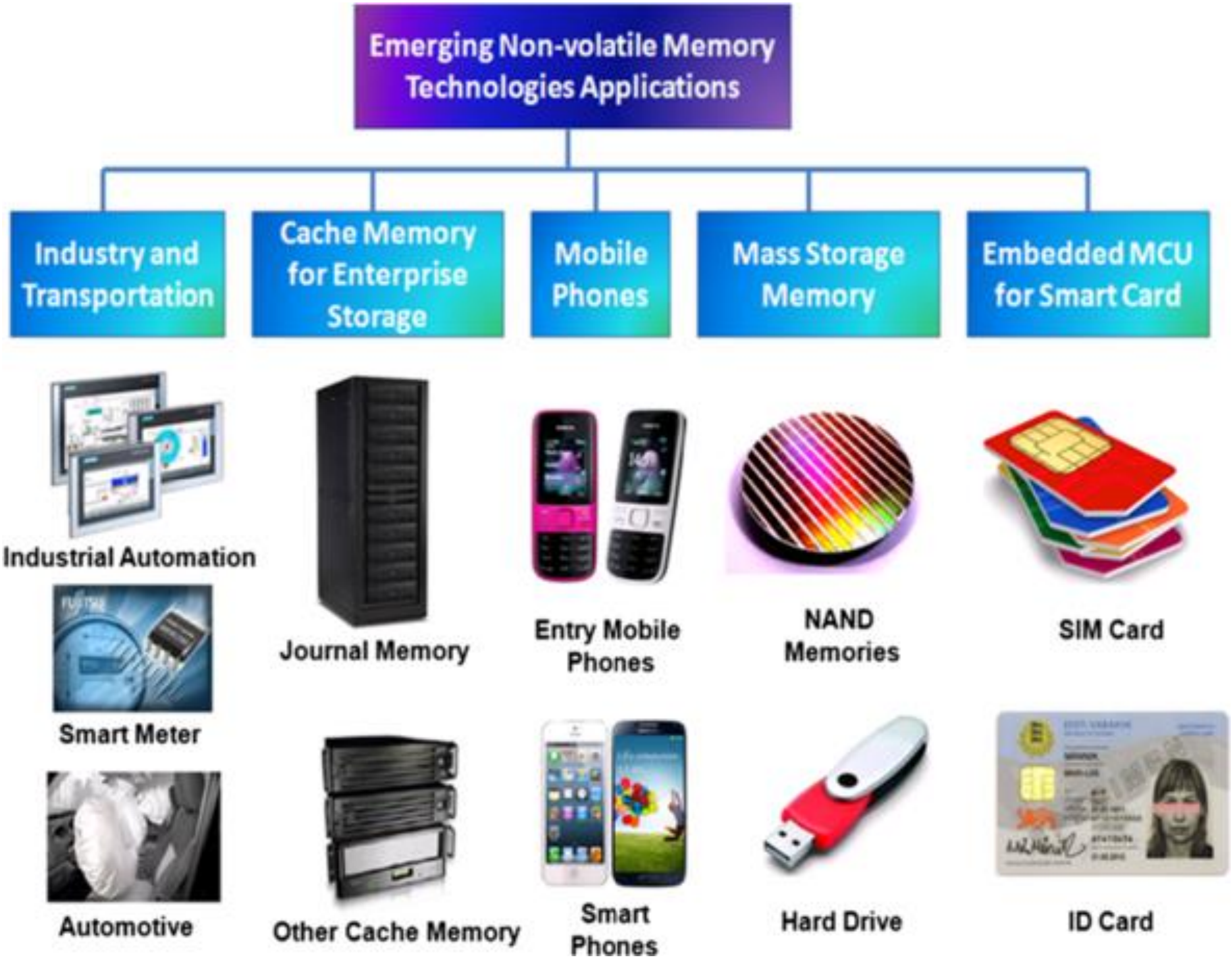


IGT on Braunschweig
Univ. substrates



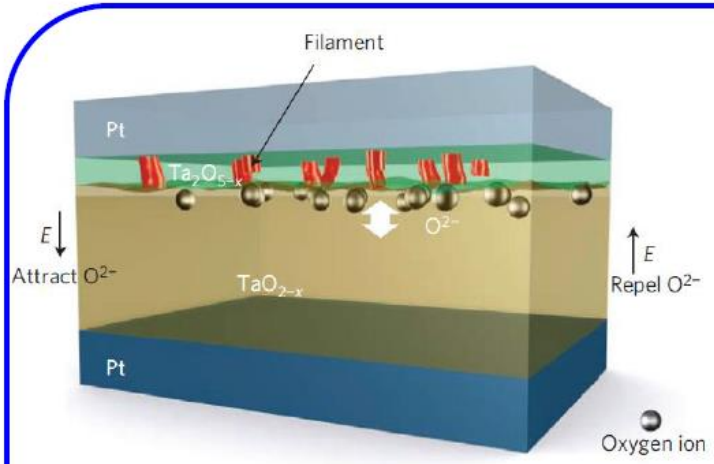
IGT on MIY patterned substrates

NVM applications in various markets

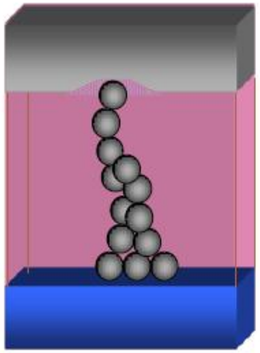


Meena et al. Nanoscale Research Letters 2014, 9:526

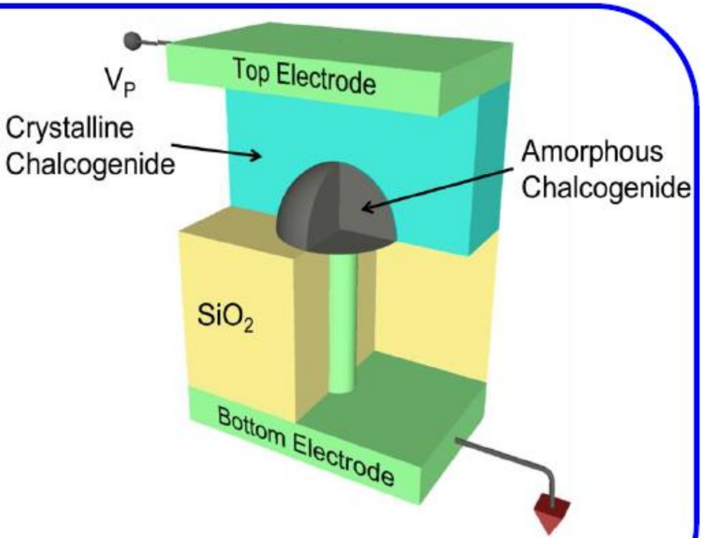
Emerging devices for memory/computing



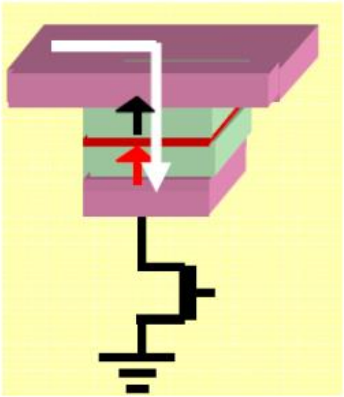
Resistive switching memory (ReRAM)



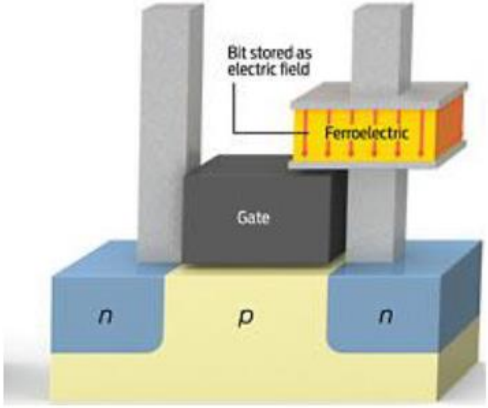
Conductive bridge memory (CBRAM)



Phase change memory (PCM)

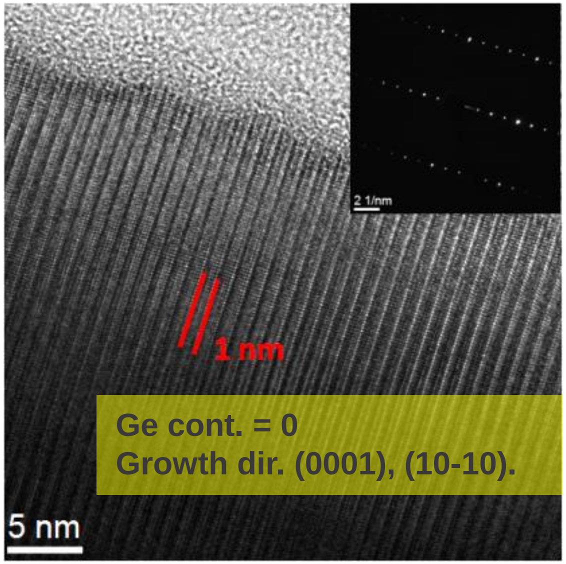


Spin-transfer torque memory (STT-RAM)

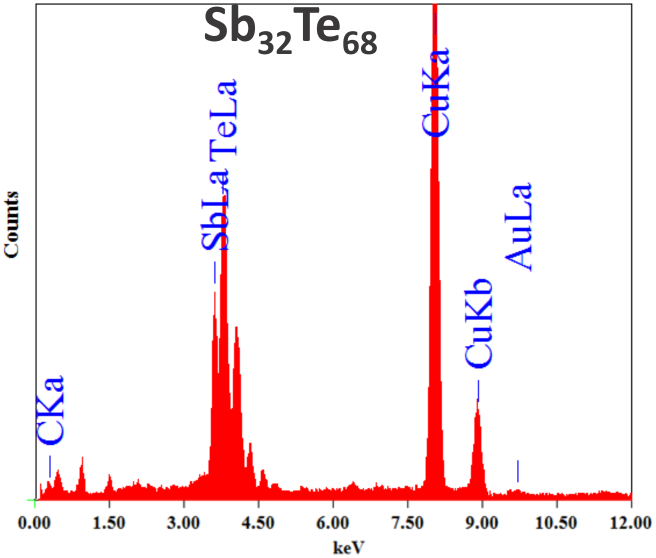


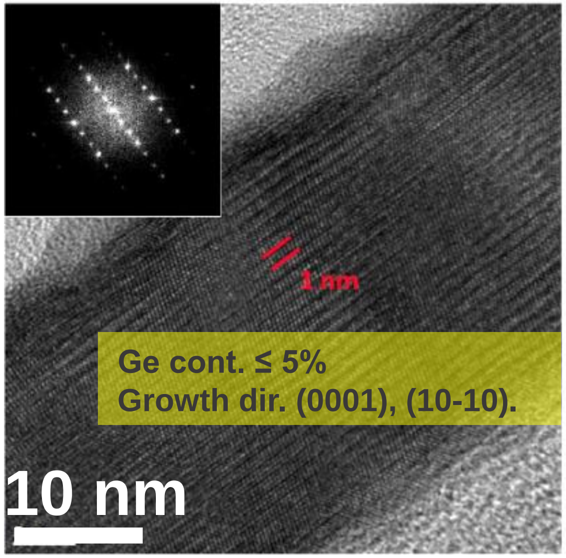
Ferroelectric memory (FeRAM)

Ge-doped Sb_2Te_3 NWS grown by MOCVD+VLS

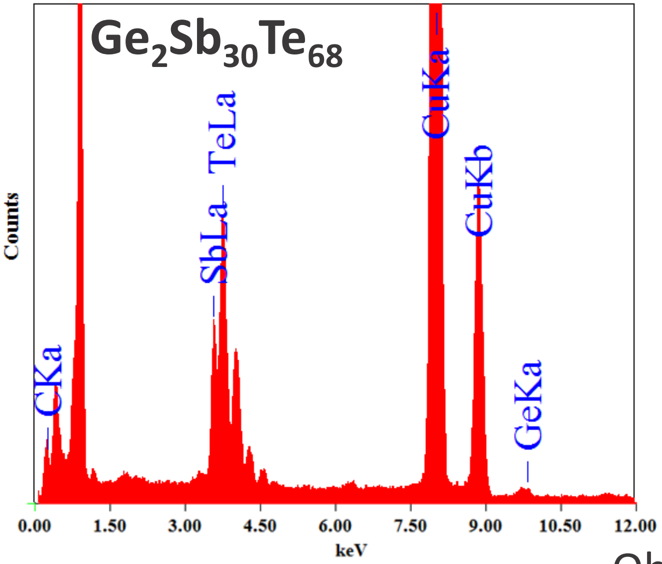


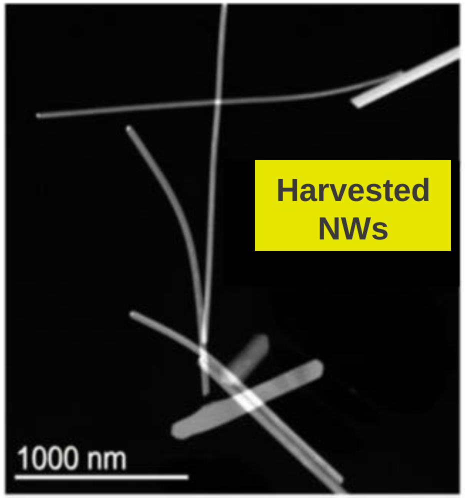
Ge cont. = 0
Growth dir. (0001), (10-10).





Ge cont. ≤ 5%
Growth dir. (0001), (10-10).





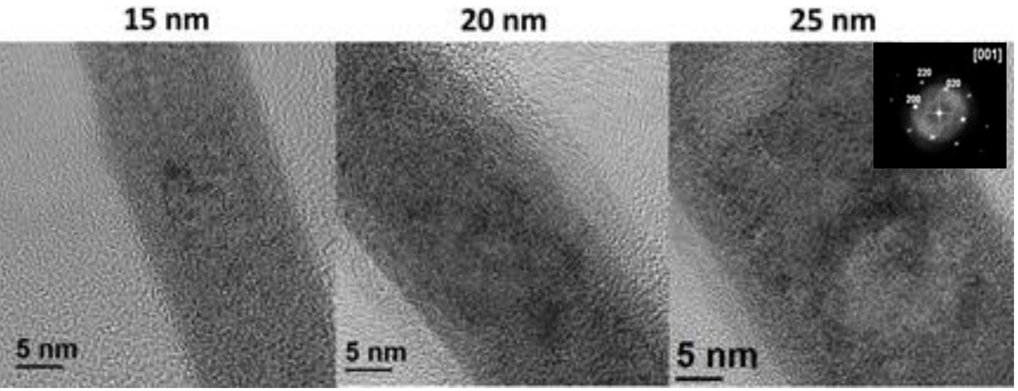
Harvested NWs

M. Longo et al., J. of Cryst. Growth 370 (2013) 323–327

Obtained with SAFC precursors

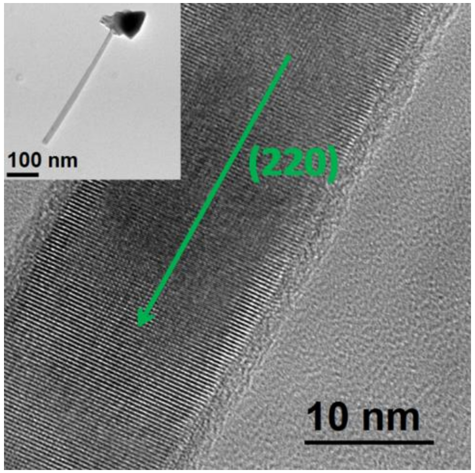
Optimised In-Sb-Te NWs on SiO_2

T=350 °C, P=750 mbar

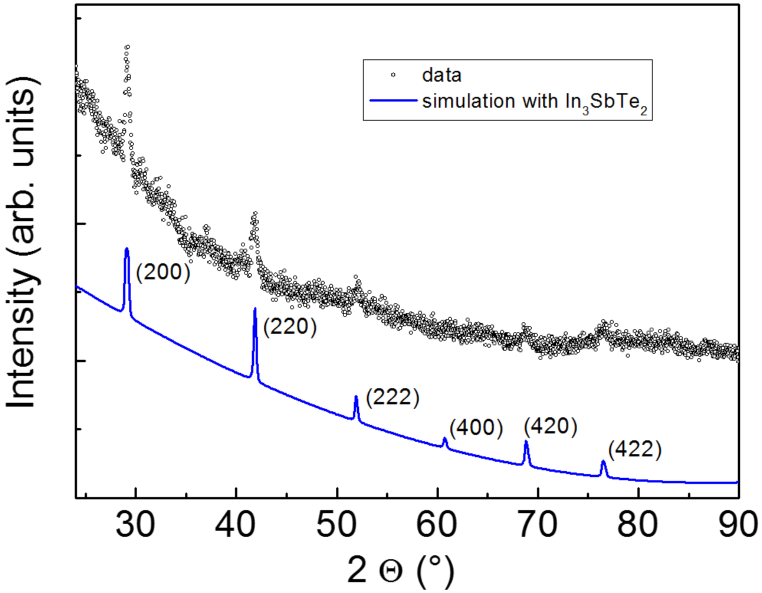


different Au precursors NPs sizes

Some amorphous inclusions in the 25 nm wide NW

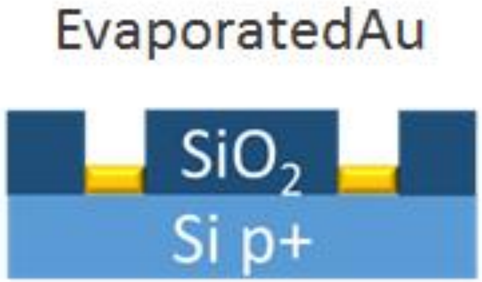


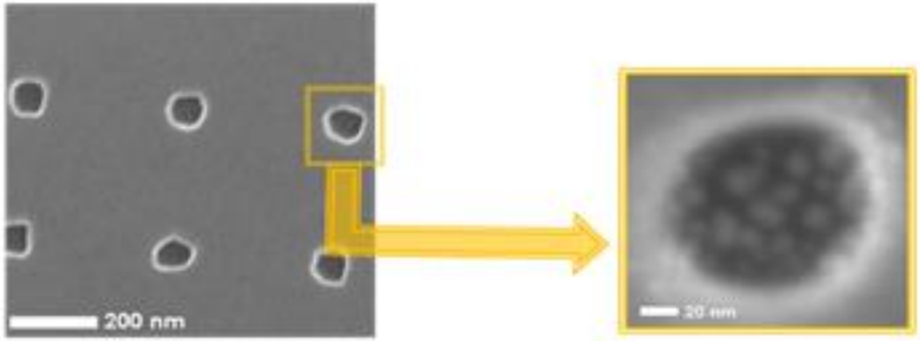
EDX: $In_3Sb_{0.4}Te_{1.3}$



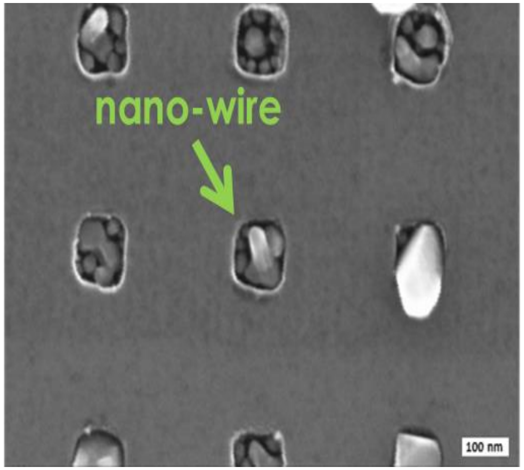
Cubic phase of $In_3Sb_1Te_2$

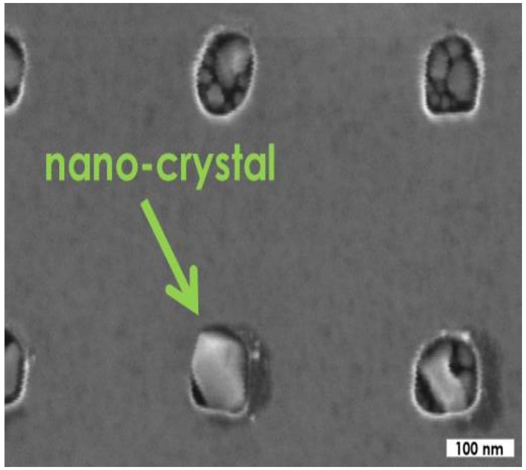
IST NW positioning on EBL+RIE-patterned templates





MOCVD

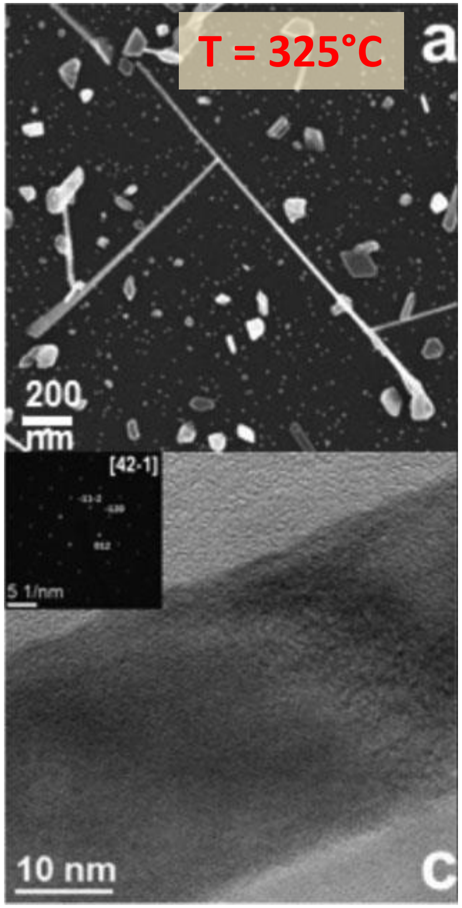




Crystals rather than NWs, formed by In-doped Sb_2Te_3 (In < 3%)

IST NW synthesis on Si(001) at 450 mbar

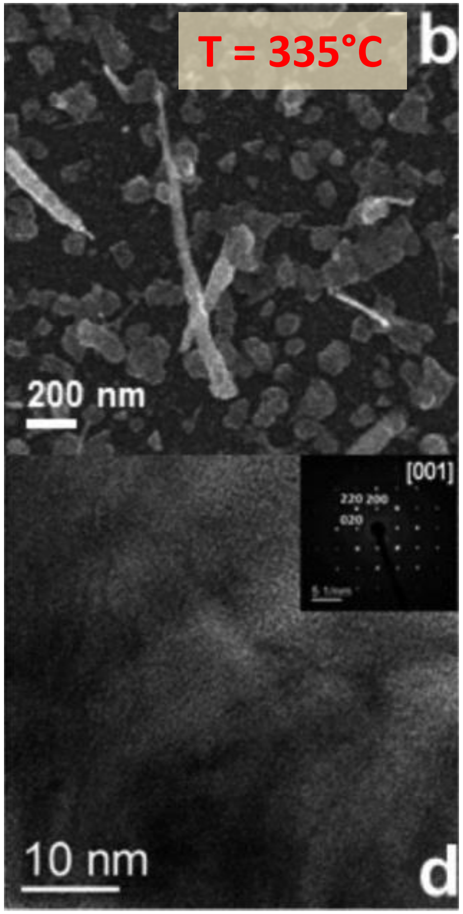
15 nm < d < 80 nm
1 µm < L < 3 µm



Thin and
regular NWs
High crystalline
quality

In–doped Sb_4Te_1
(In ~ 4.5-5.5%)

70 nm < d < 300 nm
0.5 µm < L < 1.5 µm



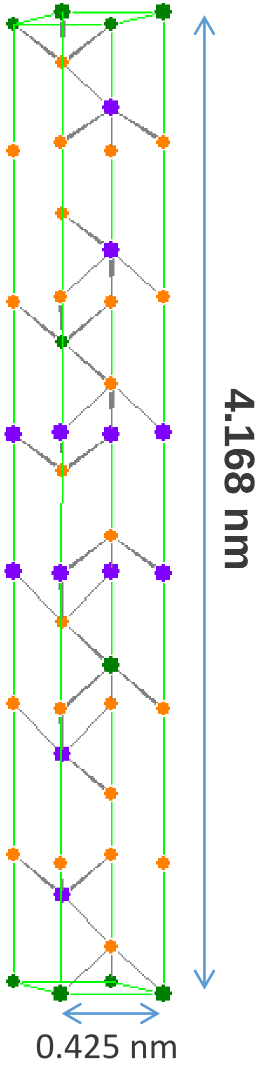
Thick and
irregular NWs
Higly defected

$In_{2.76}Sb_{0.68}Te_2$
(cubic rock salt phase)

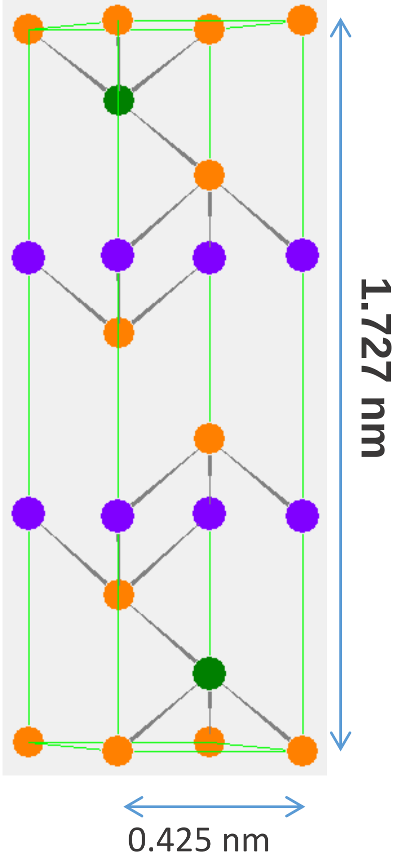
S. Selmo et al. , Phys. Status Solidi A (2016)

Phases of the Ge-Sb-Te (GST) alloys

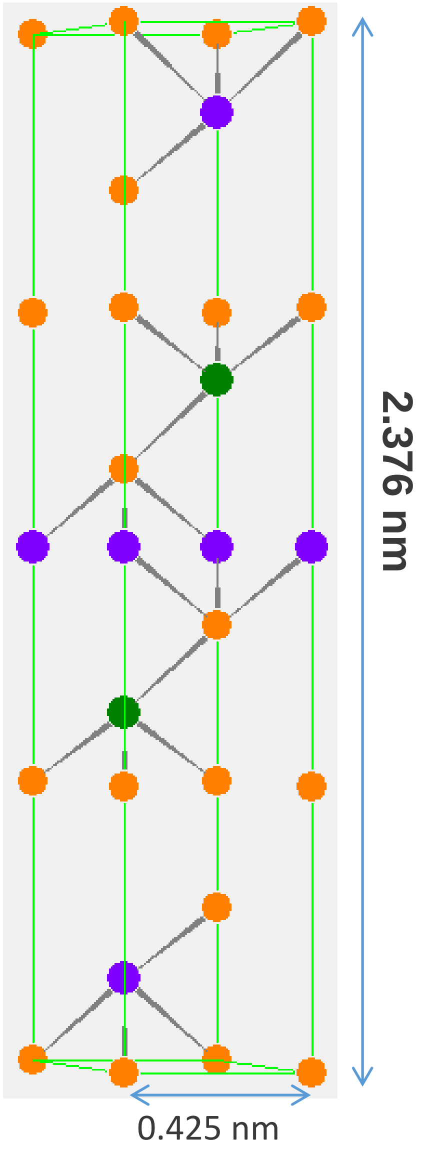
GST-124

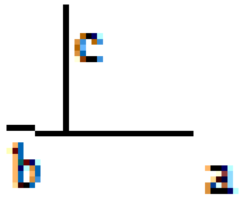


GST-225



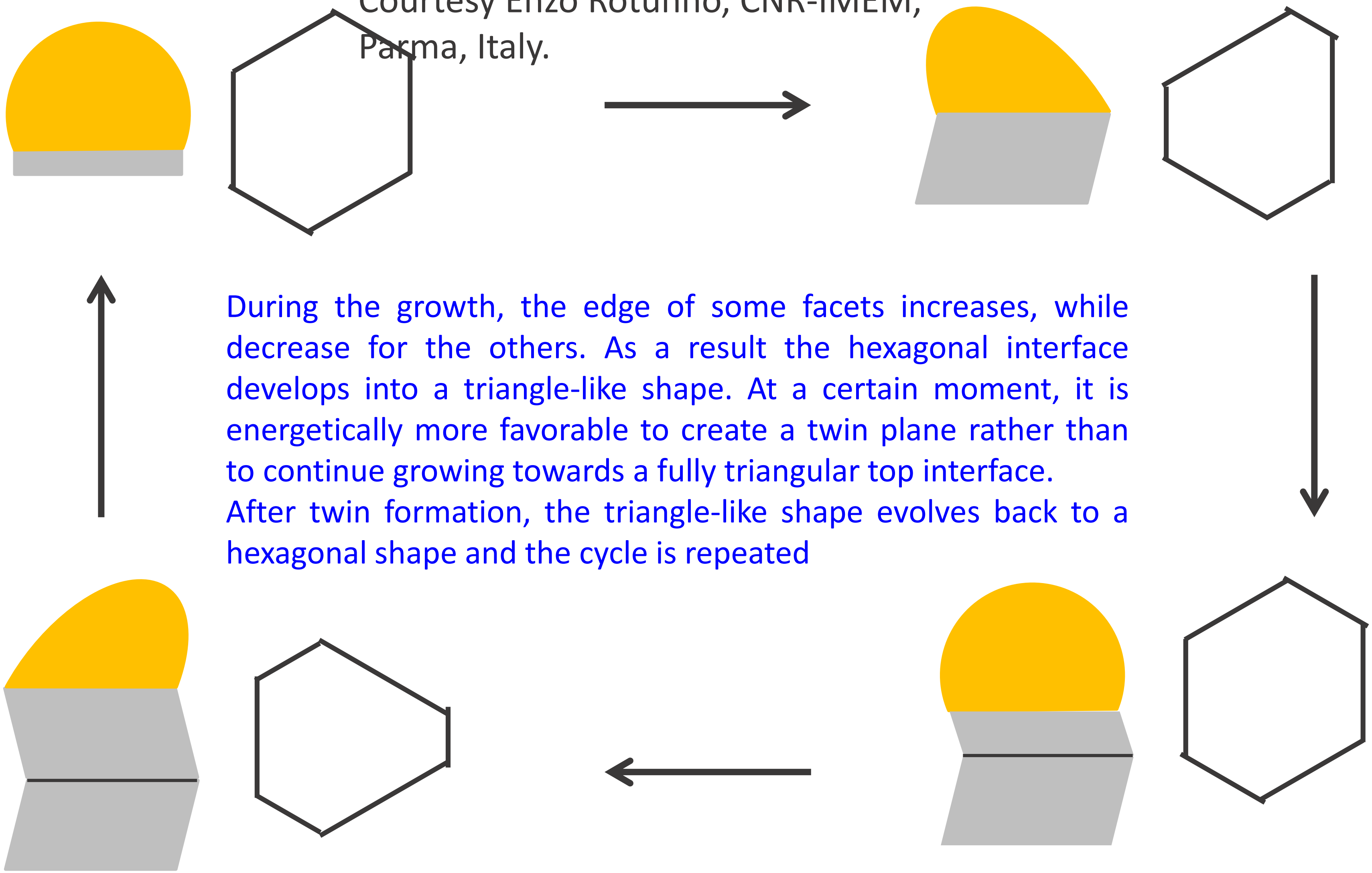
GST-147





Morphology

Courtesy Enzo Rotunno, CNR-IMEM, Parma, Italy.



During the growth, the edge of some facets increases, while decrease for the others. As a result the hexagonal interface develops into a triangle-like shape. At a certain moment, it is energetically more favorable to create a twin plane rather than to continue growing towards a fully triangular top interface.

After twin formation, the triangle-like shape evolves back to a hexagonal shape and the cycle is repeated

F. M. Davidson *et al.* J. Phys. Chem. C, 2007, 111, 2929–2935.

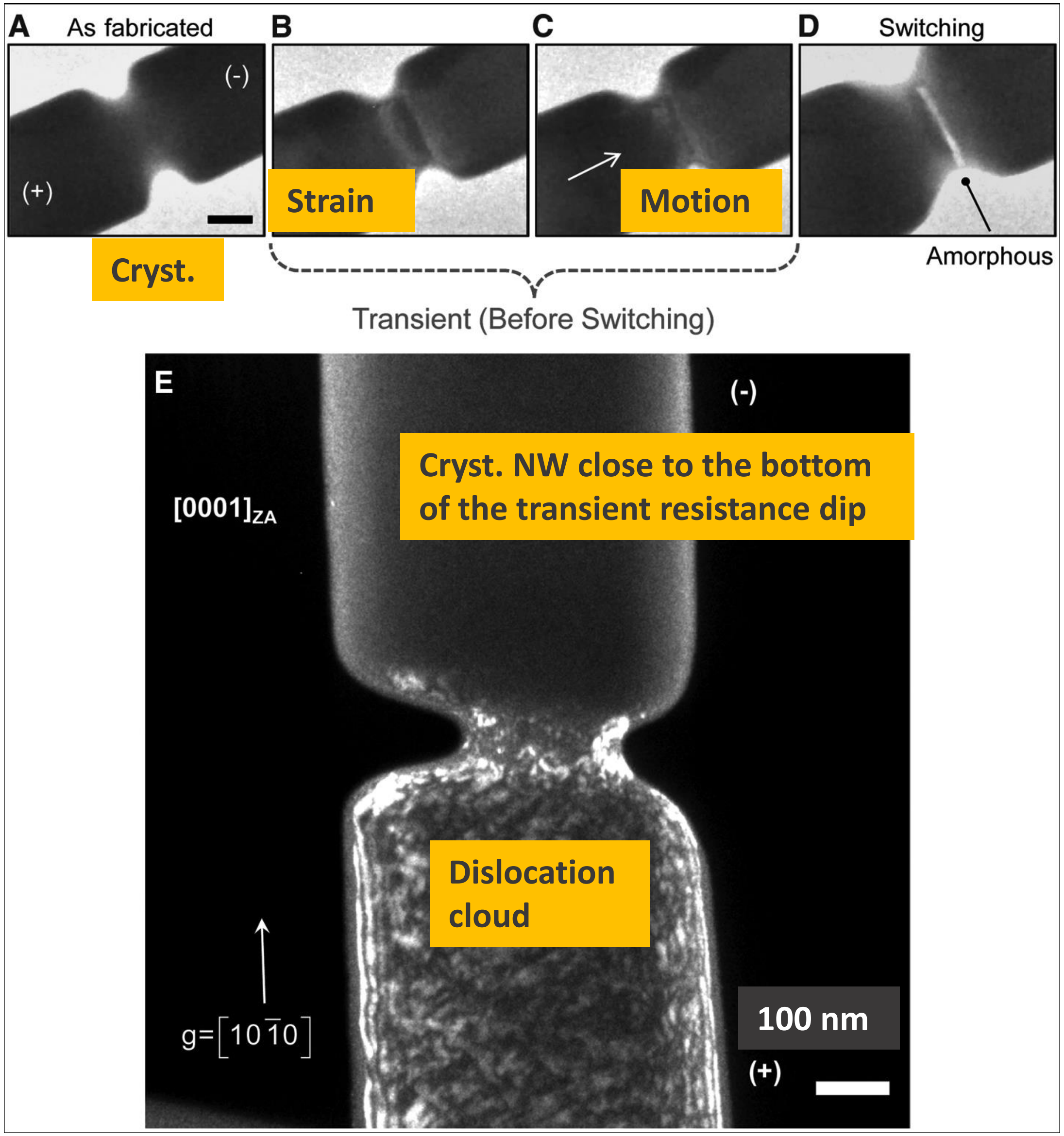
Melt quenching or dislocation jamming?

Cryst. → amorph. transitions in GST NWs, observed in-situ

Resistance "dip" just before amorphization was correlated to dislocation loops growing along the [10-10], reducing vacancies.

Dilsocations move (electrical wind forces) aligned to hole carriers, until they are stopped for heavy accumulation, inducing amorphization.

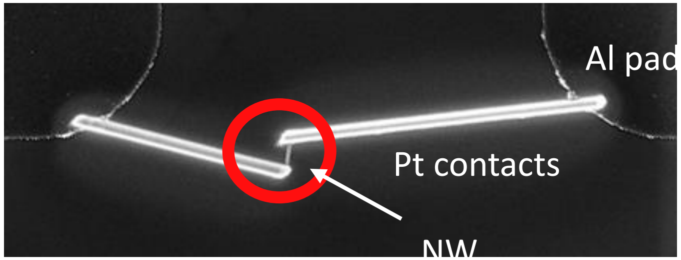
Sharp resistance increase, with bright line indicating the amorphized region and a cloud of dislocations left behind it.



S.W. Nam et al., Science, **336** (2012) 1561

Electrical analysis on single Ge-doped Sb-Te NW

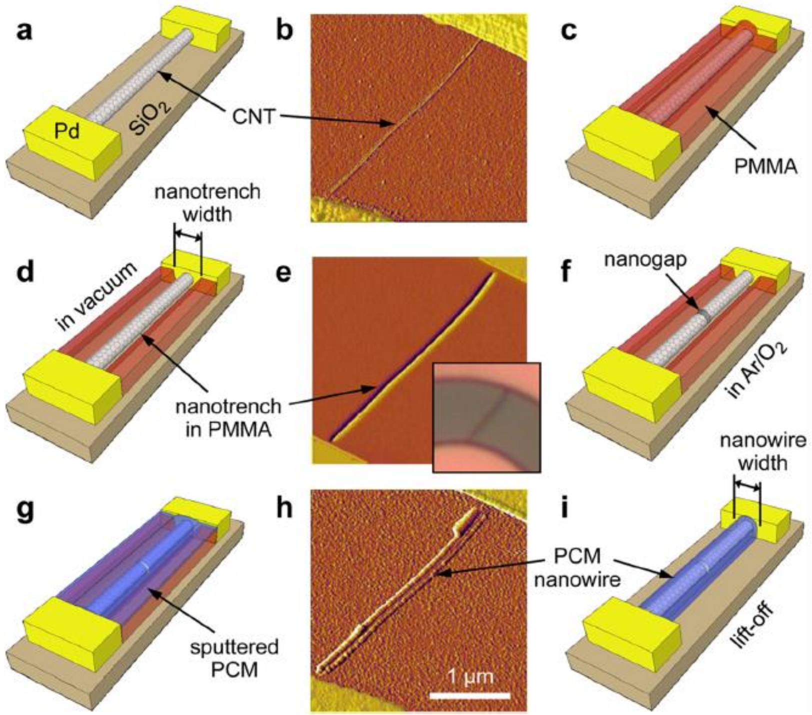
Phase change accomplished by 300 ns, 3 V pulses

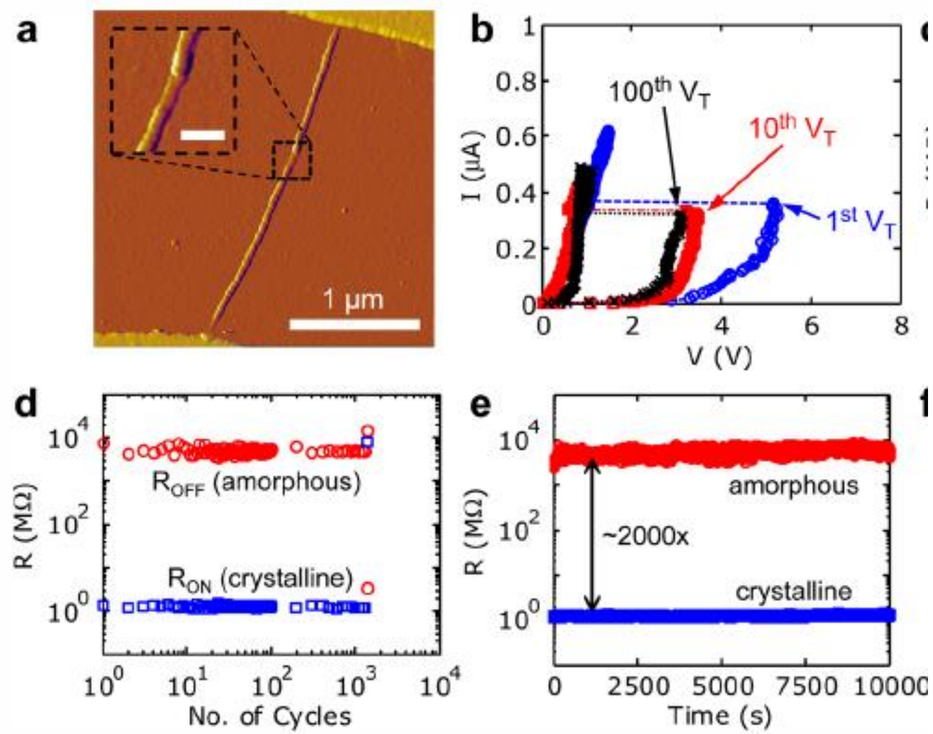


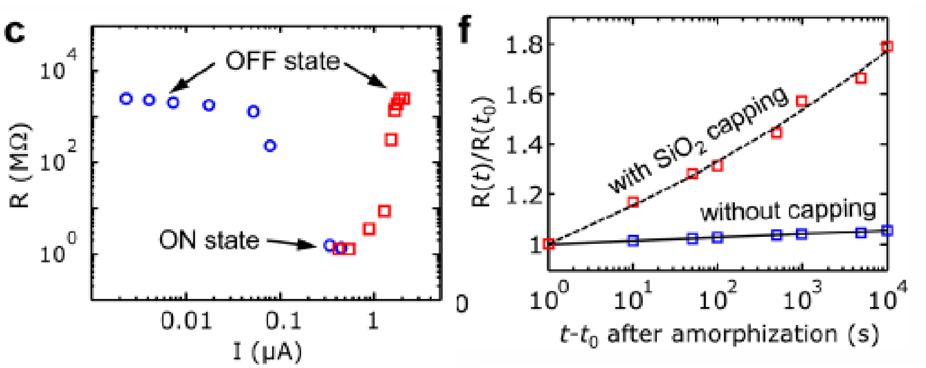
Sample	TXRF composition	Ge at.%	SET R [kΩ]	RESET R [MΩ]
#332-2H	$Ge_{0.2}Sb_3Te_{6.8}$ NWs	5.8	14.4	9.09
#392-C30	$Ge_{0.1}Sb_3Te_5$ NWs	< 1.3	2.90	0.58
#326	$Ge_{0.55}Sb_{2.66}Te_5$ NWs	14	5.73	0.27
#455-2L	Sb_2Te_3 NWs	0	25.7	-
#453-C50	Sb_2Te_3 NWs	0	21.0	-
Ref. [1]	$Ge_1Sb_2Te_4$ NWs	> 14	≈ 4	≈ 0.45
Ref. [2]	$Ge_2Sb_2Te_5$ NWs	22	≈ 10	≈ 2
Ref. [3]	Sb_2Te_3 NWs	0	≈ 33	≈ 50
Ref. [4]	Sb_2Te-line memory cells	0	≈ 10	≈ 10

[1] Longo et al., Nano Letters, 12 (2012) 1509−1515
[2] Lee et al., Physica E 40, 2474–2480 (2008)
[3] Lee et al., J. Am. Chem. Soc., 130 6252-6258 (2008)
[4] Jedema et al., NVSMW/ICMTD 2008, p. 43-45

Self aligned nanotube-nanowire PCM – litho independent







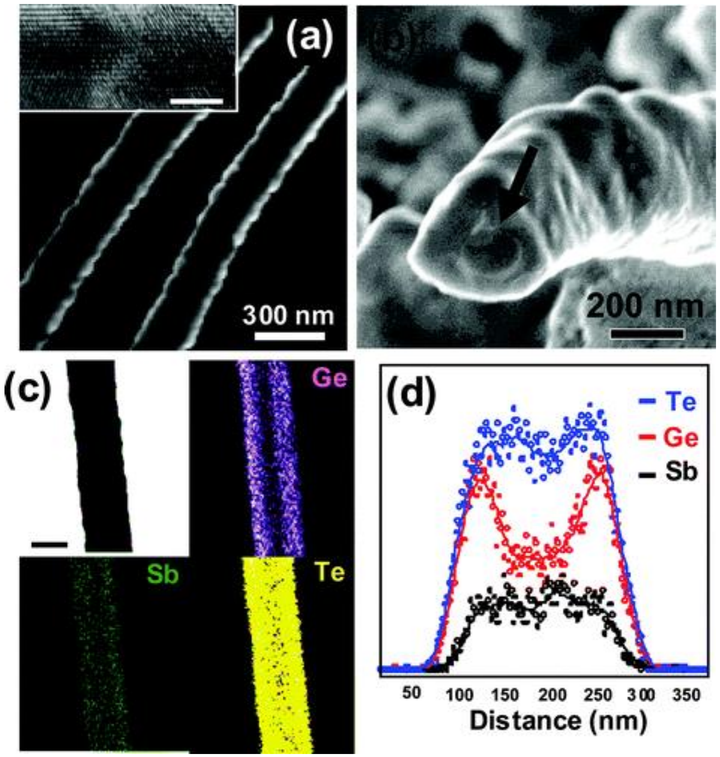
GST NW: ~ 40 nm wide, ~10 nm tall, capped by ~10 nm SiO_2

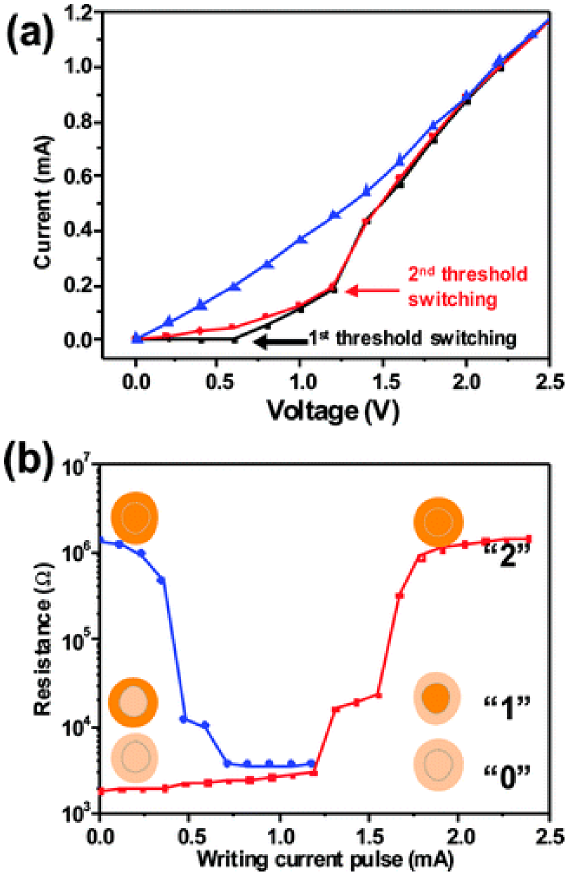
Highly scaling, ultralow prog. currents (~0.1 µA set, ~1.6 µA reset), outstanding on/off ratios (~10^3), improved endurance and stability.

F. Xiong Nano lett., **13** (2013) 464-469

Core-shell GST/GeTe NWs for multilevel PCMs

GST/GeTe Core-Shell NWs



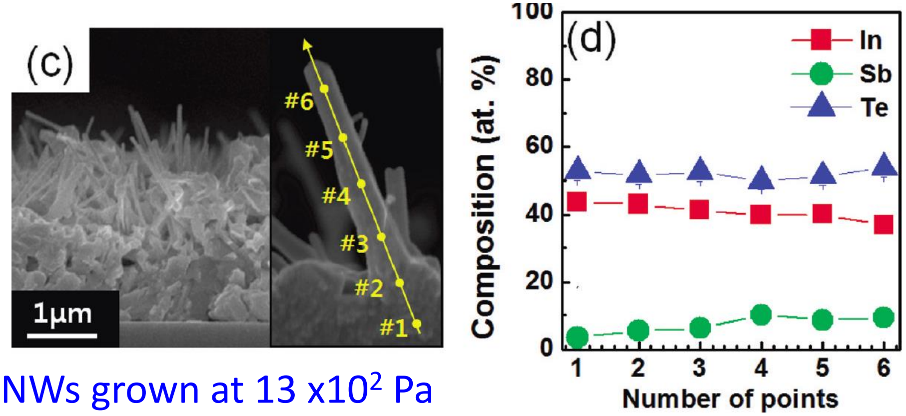


Jung et al., Nano Lett., 2008, 8 (7), 2056–2062

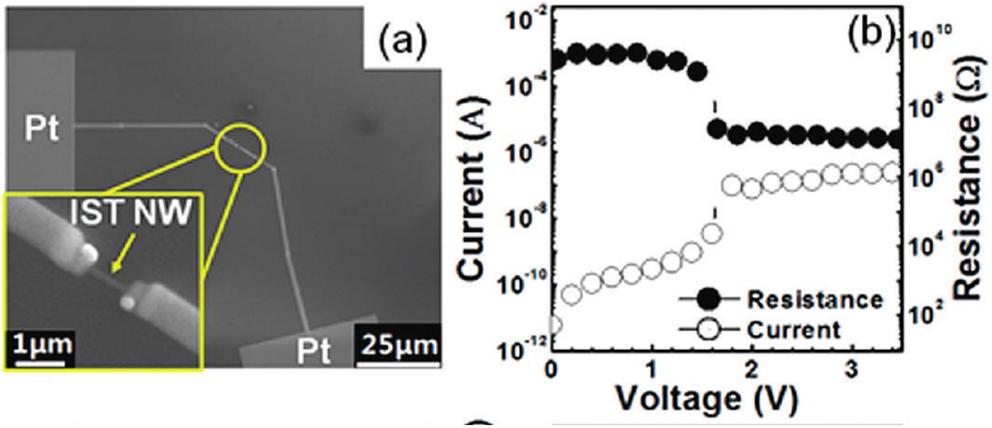
Multilevel data encoding is realized by introducing different offsets of phase transitions, in a core-shell/shell-core sequence, thus obtaining at least an intermediate, **mixed resistive state**.

In-Sb-Te NWs by MOCVD

J.K. Ahn et al., Nano Lett. 2010, *10*, 472-477

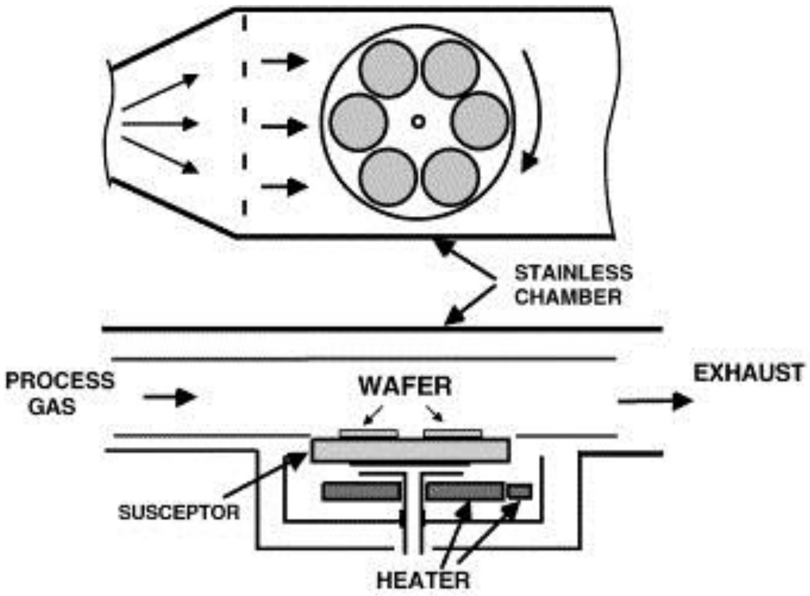


NWs grown at 13 x10^2 Pa



Sb incorporated into the InTe protrusions, grown as an IST NW. V_{Th} ~ 1.6 V

H. Tokunaga et al., J. of Cryst. Growth, 221 (2000) 616



Scheme of a multiwafer MOCVD reactor

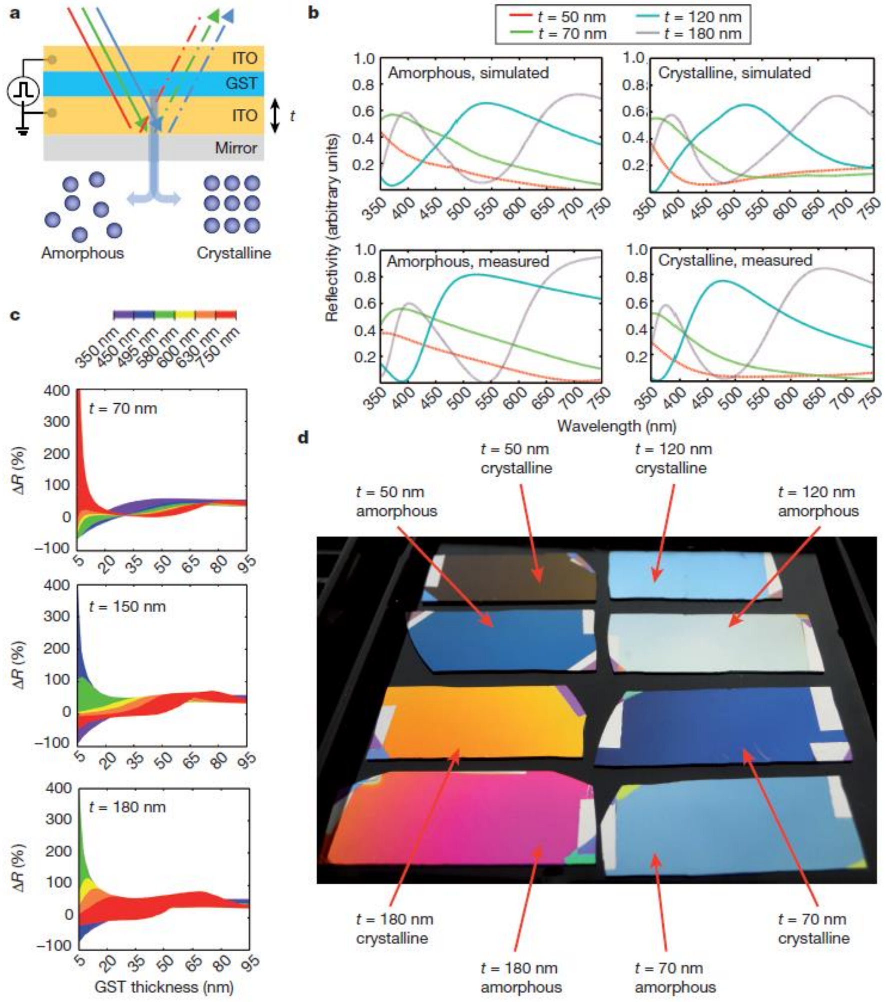
If the NW self-assembly can be controlled, along with industrial scalability of MOCVD → high exploitation of PCM scaling properties!

New functionalities for chalcogenide nanostructures

Memristors → Neuromorphic memories and computing

Thermoelectric materials

Optical on-chip memory devices



Optoelectronics

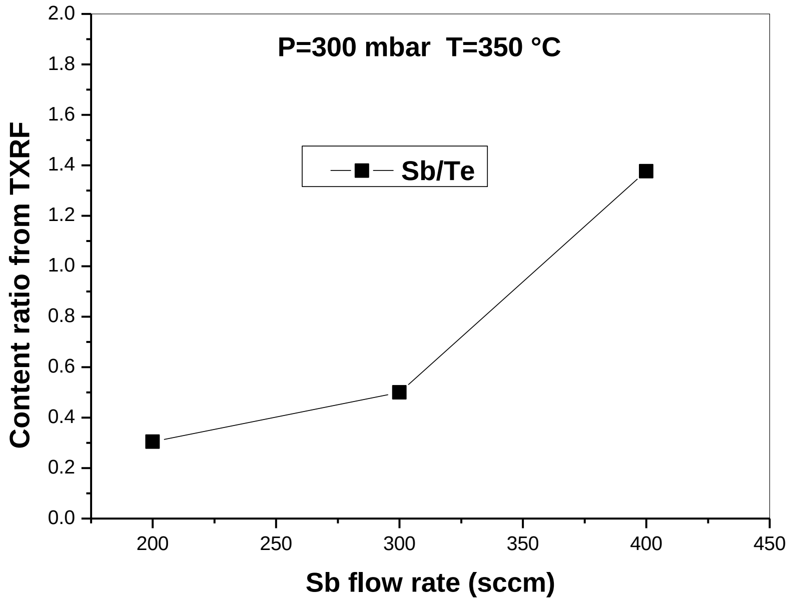
Electrically induced stable color changes in both reflective and semi-transparent modes, even in flexible films.

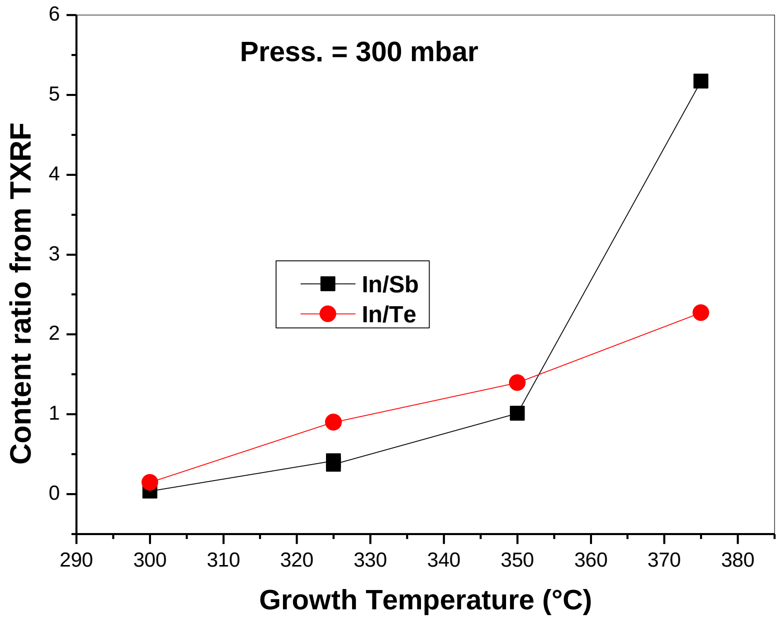
→ ultrafast displays with nm-scale pixels, semi-transparent ‘smart’ glasses, contact lenses, artificial retina devices...

P. Hosseini et al., Nat. Res. Lett., 2014

In-Sb-Te NW synthesis on Si(001)

More efficient growth → Depositions at **300 and 450 mbar** with similar trends





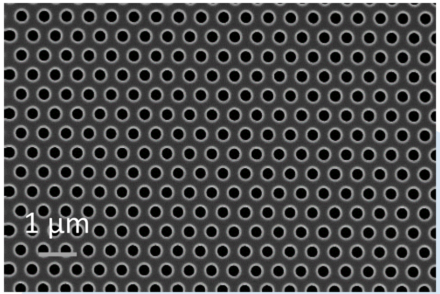
Average composition and structure dimension strongly depend on the deposition conditions

⬇

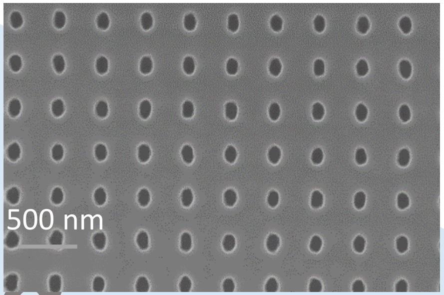
Growth of NWs with different morphology and compositions

Templates for NWs arrays

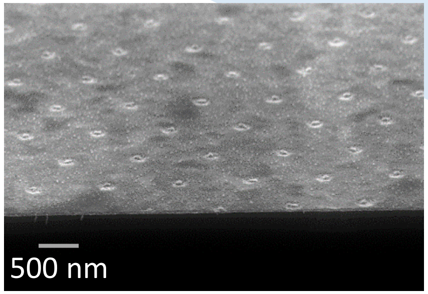
No Au for SAG
UV-litho (@ FZJ)



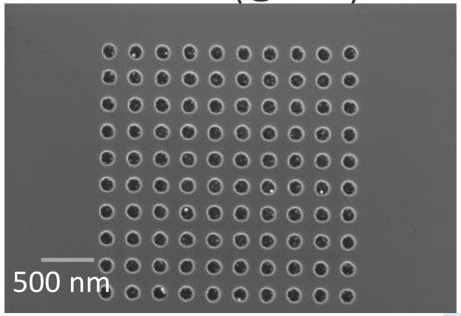
VLS/SAG on $CoSi_2$
UV-litho



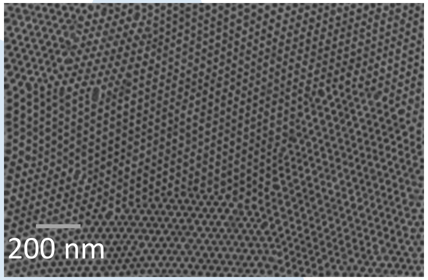
Au film for VLS
NI-litho
(@ Braunschweig Univ.)



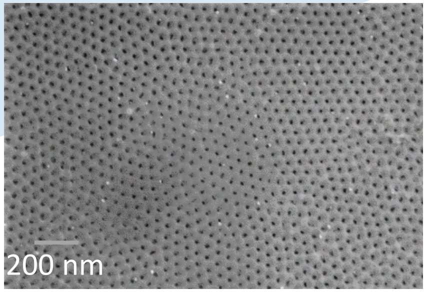
Au NPs for VLS
EB-litho (@CNR)



Au film for VLS
BC-litho (@CNR)



Au NPs for VLS
AAO (custom made @ InRedox)



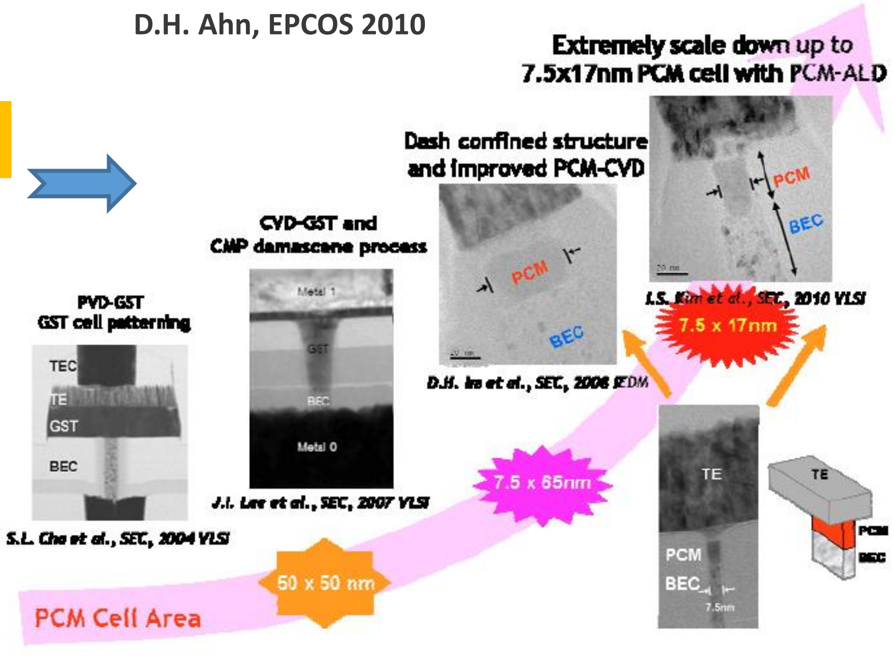
Increased density

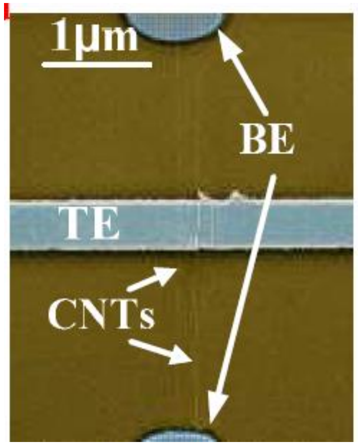
VLS = Vapor Liquid Solid
SAG = Selective Area Growth
NI = Nano Imprinting
BC = Block-Copolymer
AAO = Anodic Aluminum Oxide
EB = Electron beam
NP = nanoparticles

Scaling of PCM cells

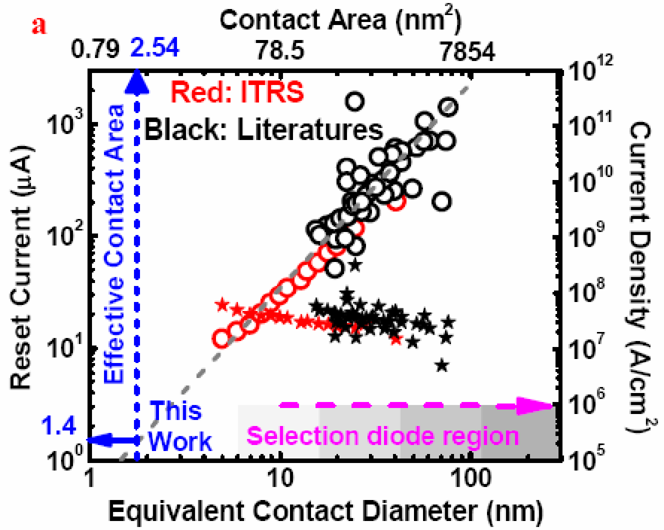
D.H. Ahn, EPCOS 2010

Use of CVD-based techniques

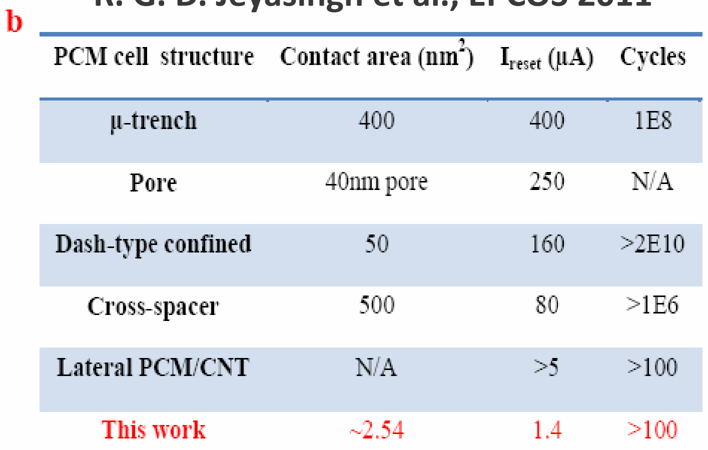




Cross-point PCM cell



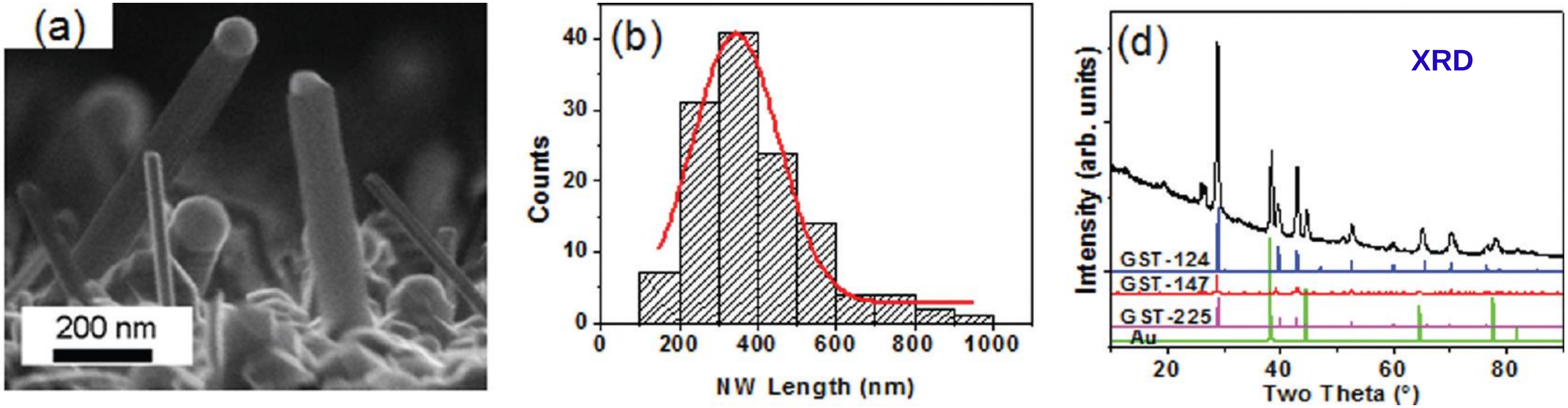
R. G. D. Jeyasingh et al., EPCOS 2011

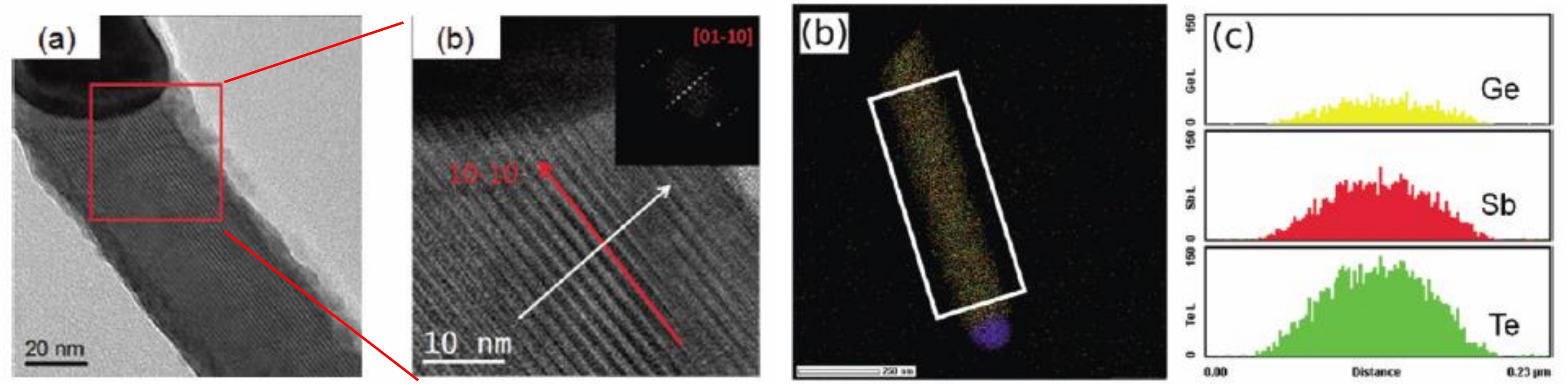


b

PCM cell structure	Contact area (nm^2)	I_{reset} (μA)	Cycles
µ-trench	400	400	1E8
Pore	40nm pore	250	N/A
Dash-type confined	50	160	>2E10
Cross-spacer	500	80	>1E6
Lateral PCM/CNT	N/A	>5	>100
This work	~2.54	1.4	>100

Optimized $Ge_1Sb_2Te_4$ NWs by MOCVD + VLS

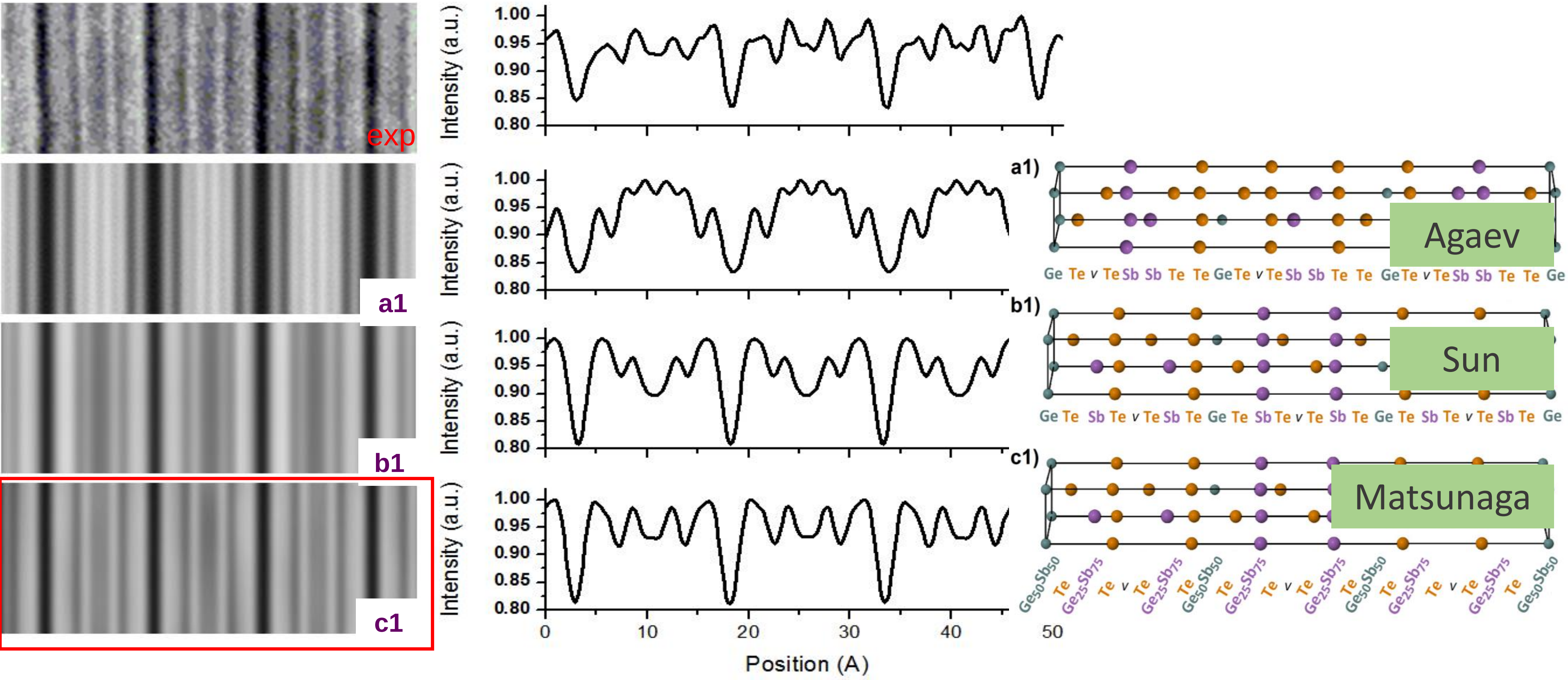




M. Longo et al., Nano Lett., 12 (2012) 1509

$Ge_1Sb_2Te_4$ NWs: rhomboedral phase and growth directions that correspond to the [1 0 0] and [1 1 2] of the rock-salt cubic structure. Homogeneous alloy.

Simulation of Z contrast (STEM-HAADF) images

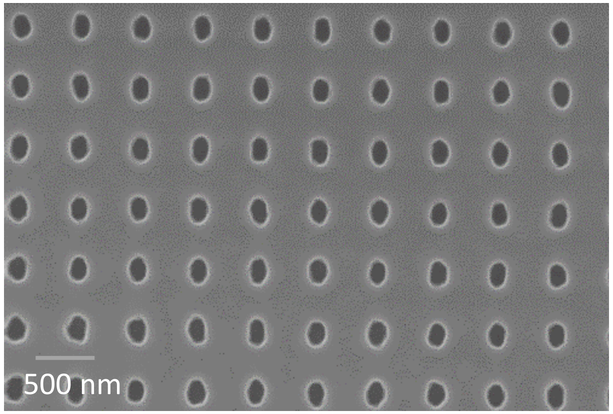


HAADF-STEM and simulations demonstrate that GST-124 NWs crystallize with mixed occupation in the Ge/Sb planes, despite the adverse theoretical predictions

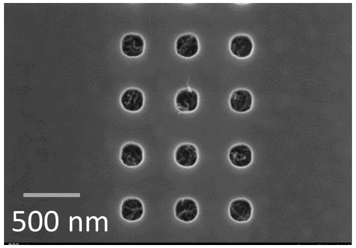
E. Rotunno et al., Nanoscale, 2013, 5, 1557

IGT NWs arrays: Ultraviolet lithography on $CoSi_2$ film

$CoSi_2$ film for VLS /SAG



IST

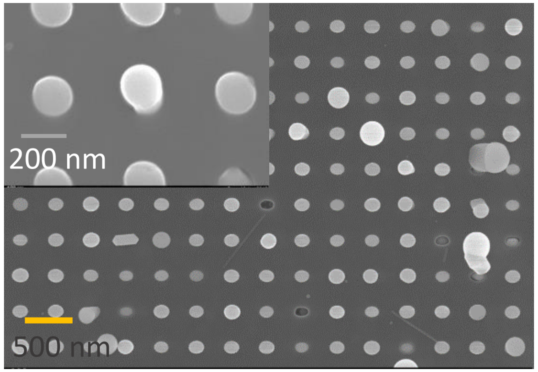


IST
No/poor growth
(Ge contamination?)

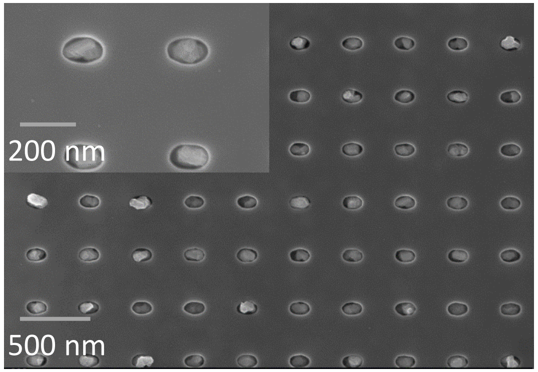
IGT

nano-pillars

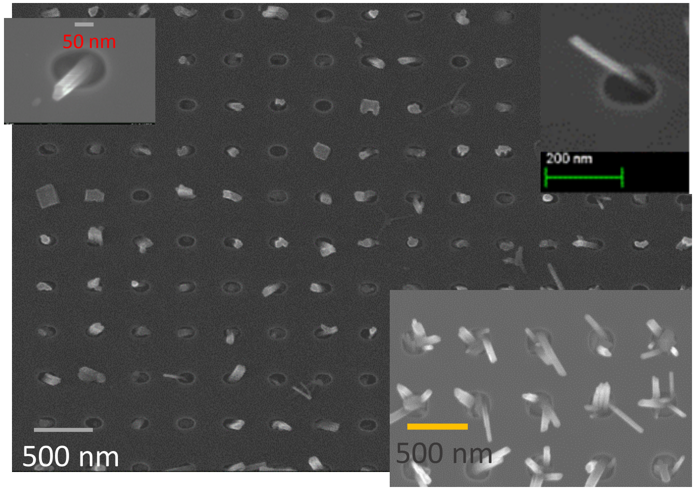
“Mushroom”-like



“Crystal”-like



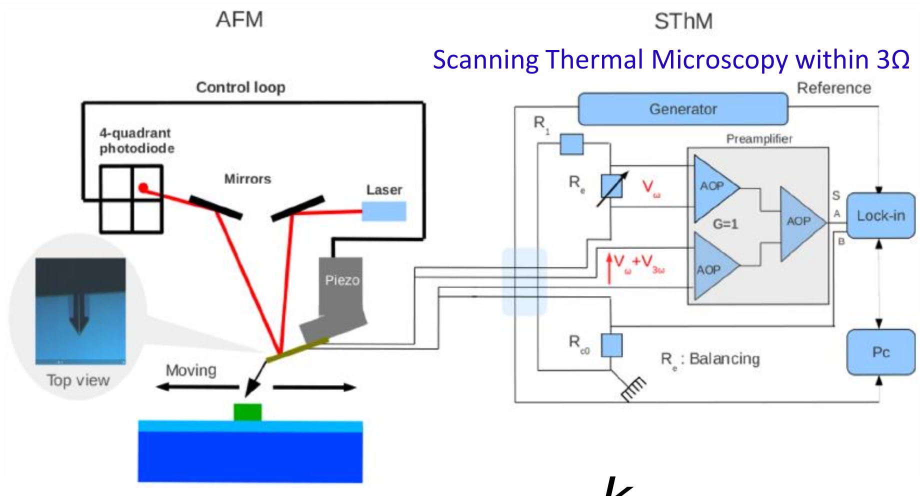
“Wire”-like

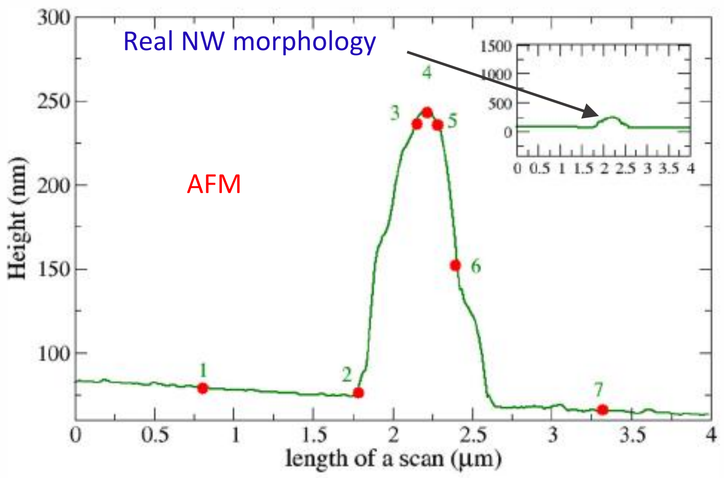


IGT

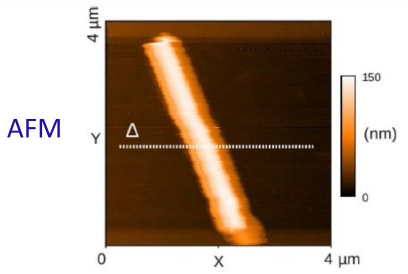
- **Selective IGT growth, including NWs**
- **Composition and morphology control**

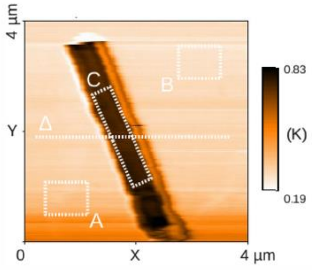
Thermal conductivity of a Sb_2Te_3 phase change NW



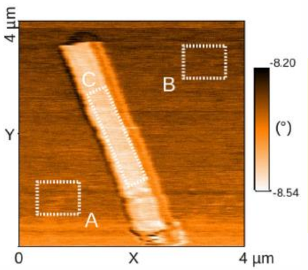


$$k_{Sb_2Te_3\text{-}NW\text{-}c\text{-}axis} = 0.93 \pm 0.1\,\mathrm{W.m^{-1}.K^{-1}}$$





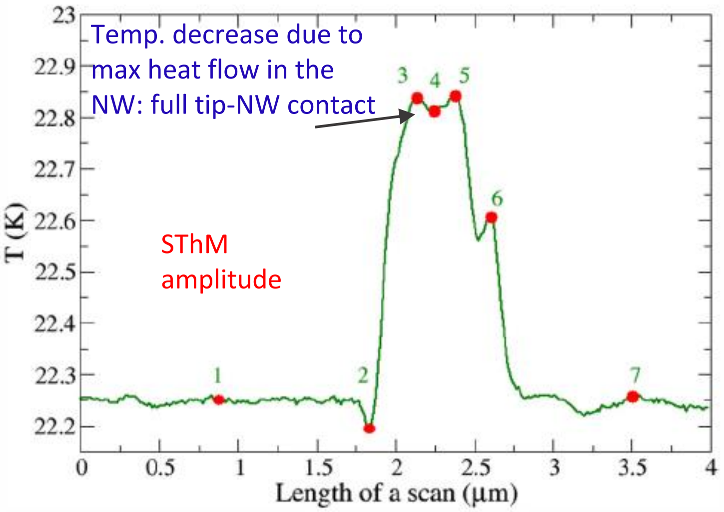
SThM amplitude



SThM phase

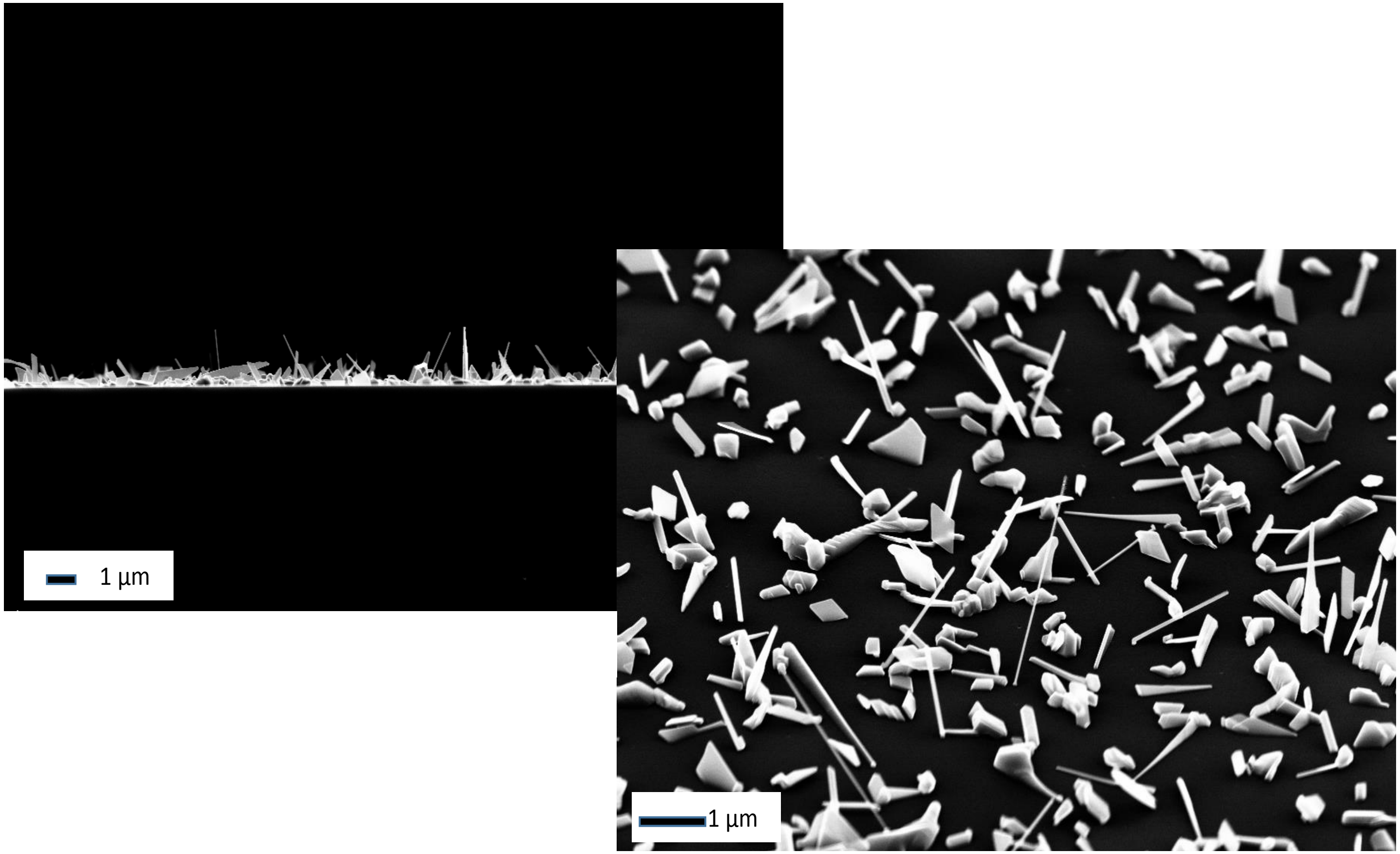
ighted as indicated in the article. Reuse ... is subject to the terms at: http://

New method without NW connection or specific configuration



A. Saci et al., Appl. Phys. Lett., 104 (2014) 263103

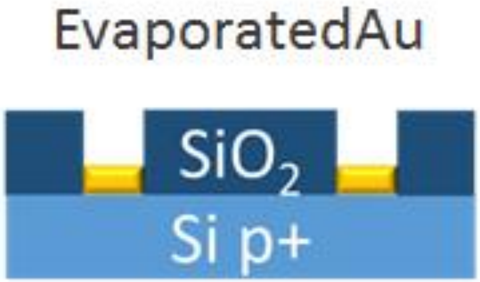
Higher precursor concentration - Sb_2Te_3 NWs growth

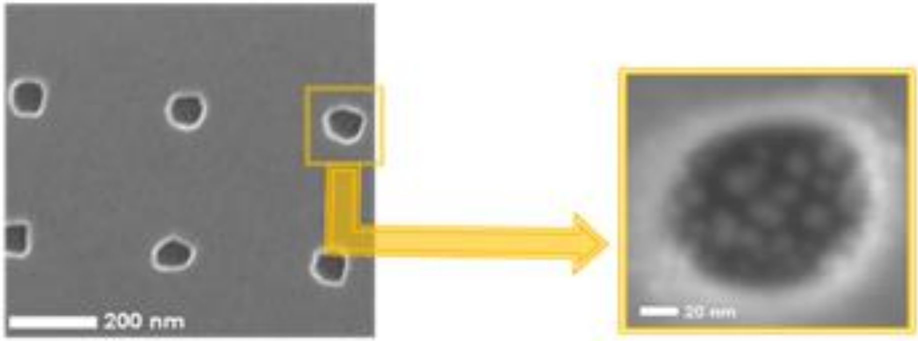


The increase of the precursor concentration increases the NW density and the crystal clusters.

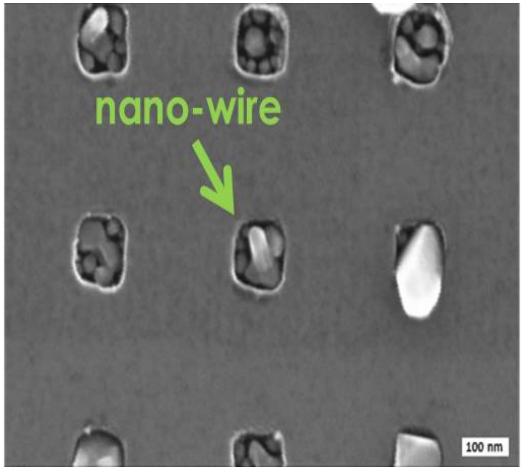
Max aspect ratio of the NWs (length/cross section) is ~ 80.

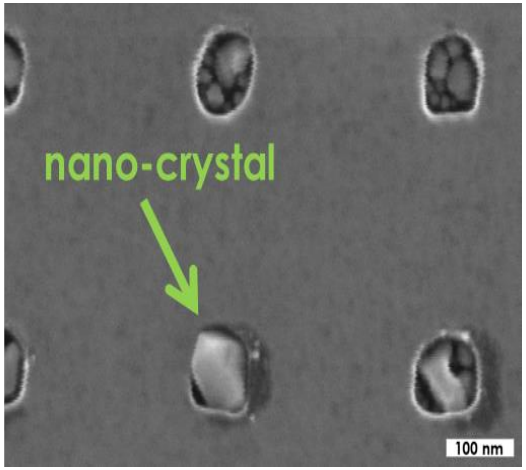
IST NW positioning on EBL+RIE-patterned templates





MOCVD

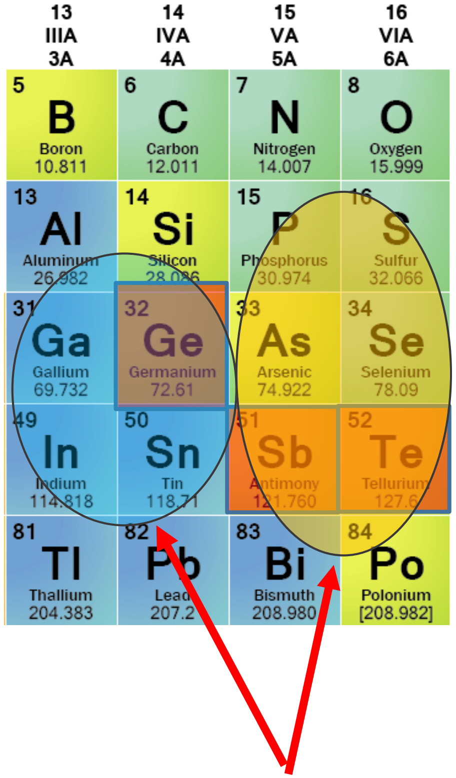




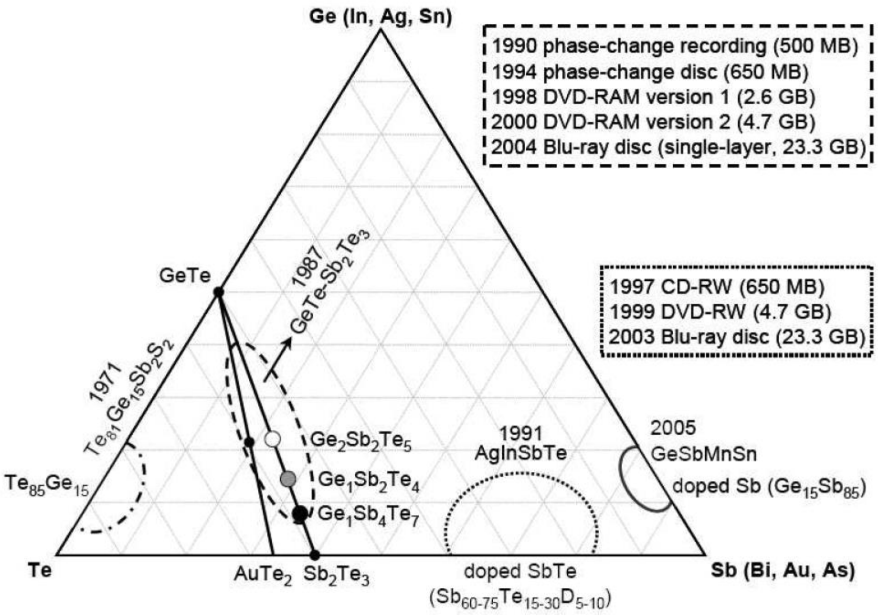
Crystals rather than NWs, formed by In-doped Sb_2Te_3 (In < 3%)

Phase change materials for NWs

M. Wuttig and N. Yamada, Nature Materials, 2007



Chalcogenides: group VI combined with group III-IV-V elements



Melting Temperature

Crystallization rate

Requirements

Table I. Scaling of phase change memory properties.

Material Property	Influence on Phase Change Memory Device	Scaling Behavior
Crystallization temperature T_x	Set power	Good
Melting temperature T_m	Reset power	Good
Crystallization speed	Data rate and set power	Depends
Thermal conductivity (amorphous and crystalline)	Set and reset power	Good
Threshold voltage	Set voltage/power	Good

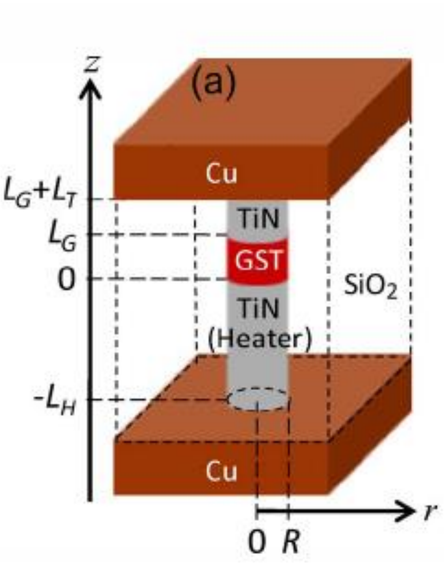
Thermal properties of phase change NWs

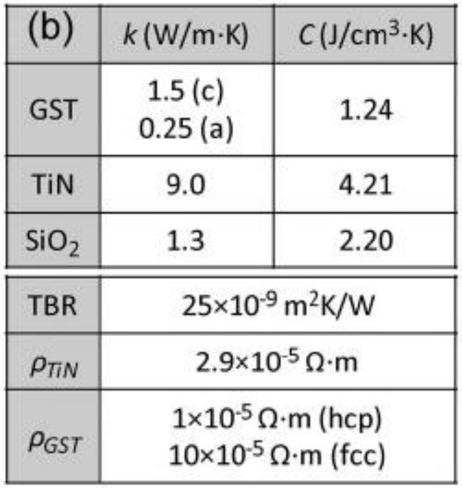
B. Piccione et al., Philosophical Magazine, 2013

$$I = 2\pi\sqrt{\frac{2k\Delta T}{\rho}\frac{r^2}{L}}$$

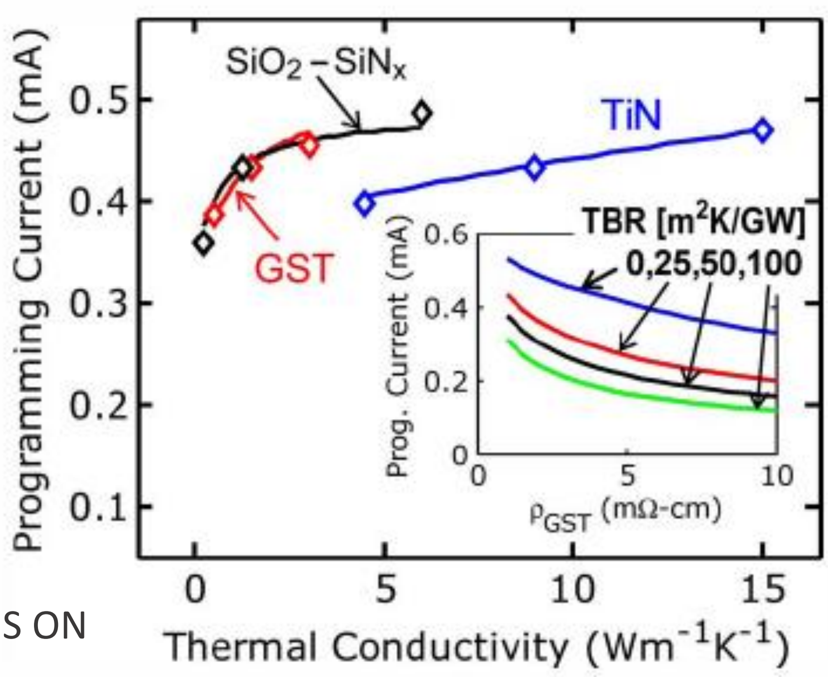
k = NW thermal conductivity
ρ = electrical resistivity
r = radius of the NW
I = writing current

TBR = Thermal Boundary Resistance at the NW /other material interface





(b)	k (W/m·K)	C (J/cm^3·K)
GST	1.5 (c) 0.25 (a)	1.24
TiN	9.0	4.21
SiO$_2$	1.3	2.20
TBR	25×10^{-9} m^{2}K/W	
ρ_{TiN}	2.9×10^{-5} Ω·m	
ρ_{GST}	1×10^{-5} Ω·m (hcp) 10×10^{-5} Ω·m (fcc)	

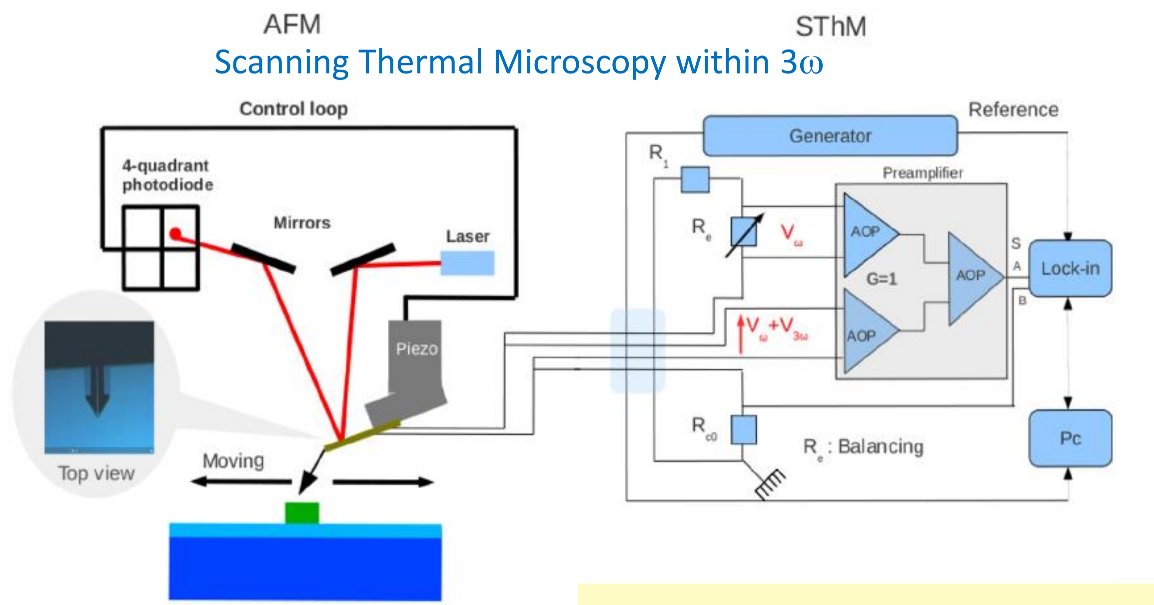


I.R. Chen et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, 2009

Low k, TBR and ρ favour lower programming currents

Scanning Thermal Microscopy (SThM)

Scanning Thermal Microscopy within 3ω



Palladium strip on the AFM tip, acting as a heater and a thermometer.

Periodic heat flux $j_0 \cos(2\omega t)$ generated in the Pd strip diffuses mainly in the probe and the rest in the investigated surface.

$I(\omega)$ → $V(3\omega)$ → T_{avg} in the strip → 3D heat transfer model → R_T

Average strip temp. (in contact with the NW) depends on:

i) probe thermal impedance (measured)

ii) contact resistance between the probe and the NW surface (measured);

iii) contact resistance between the NW and the substrate (Diffuse Mismatch model);

iv) thermal impedance of the [NW+SiO_2 layer + Si substrate] system (Finite Element method).

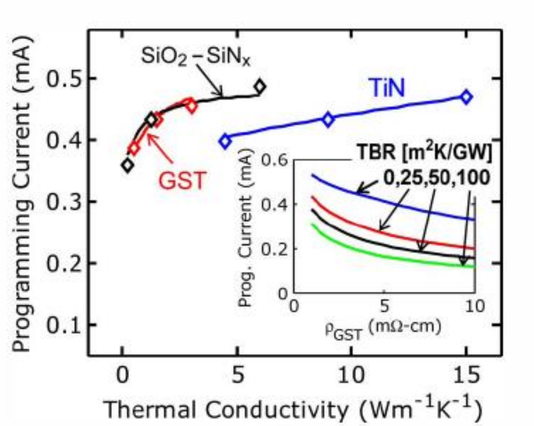
A. Saci et *al*., Appl. Phys. Lett., 104 (2014) 263103

NW size dependent thermal resistance

B. Piccione et al., Philosophical Magazine, 2013

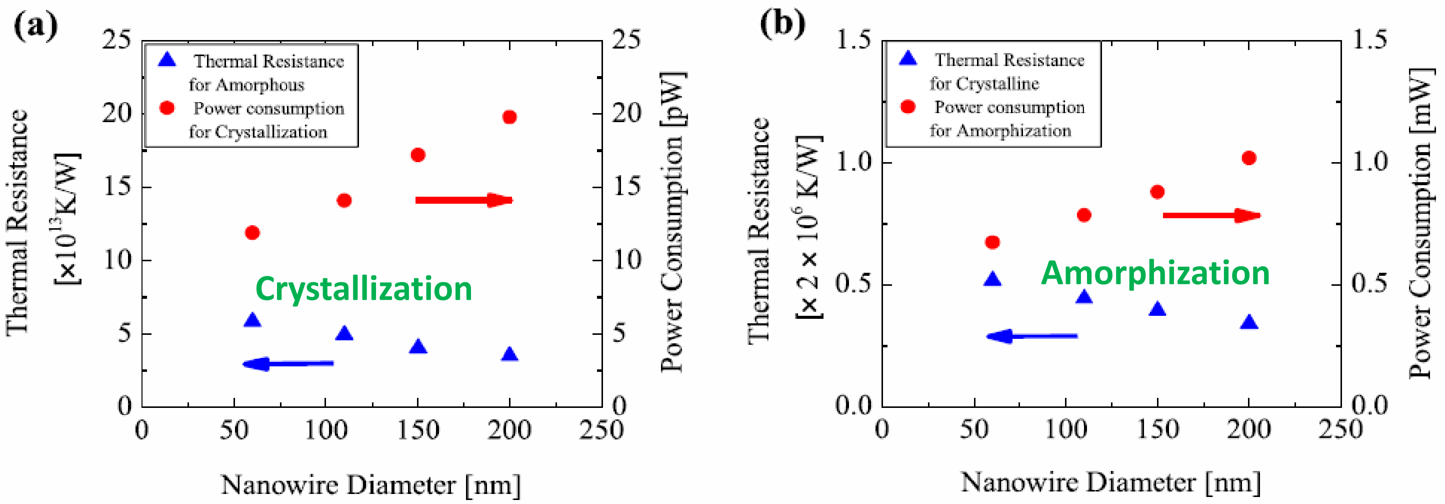
$$I = 2\pi\sqrt{\frac{2k\Delta T}{\rho}\frac{r^2}{L}}$$

k = NW thermal conductivity
ρ = electrical resistivity of the NW
r = radius of the NW
I = writing current



I.R. Chen et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, 2009

40 nm In_2Se_3 NWs encapsulated in 400 nm thick SiO_2

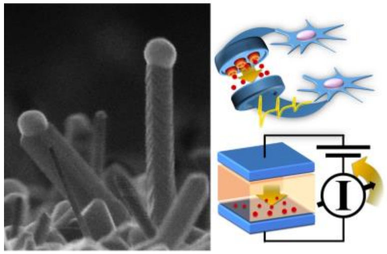


Jin et al., J. Appl. Phys. 113, 164303 (2013)

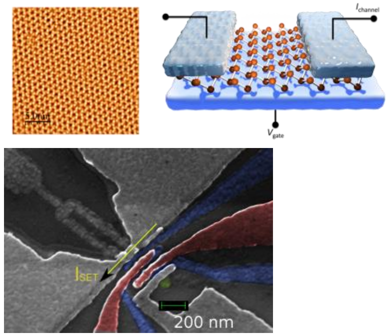
Low k, low TBR and high ρ favour lower programming currents

Branch of Agrate (MDM Laboratory)

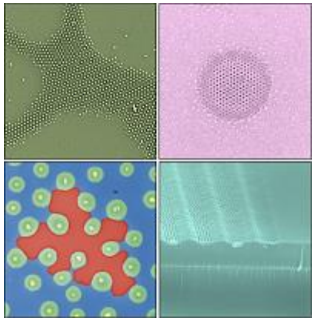
Research topics



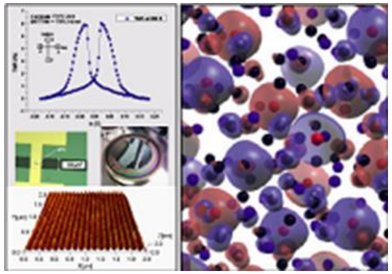
Nanoscaled materials and devices for non-volatile memories, neuromorphic systems and neuroelectronics



Low dimensional materials and devices



Self-Assembled Materials for Nanotechnology



Magnetic and multifunctional materials for spintronics and microsystems

Staff: ~40 researchers
400 m² lab with
100 m² clean room class 1000

http://www.mdm.imm.cnr.it/home.html

The FP7-SYNAPSE Project (2012-15)

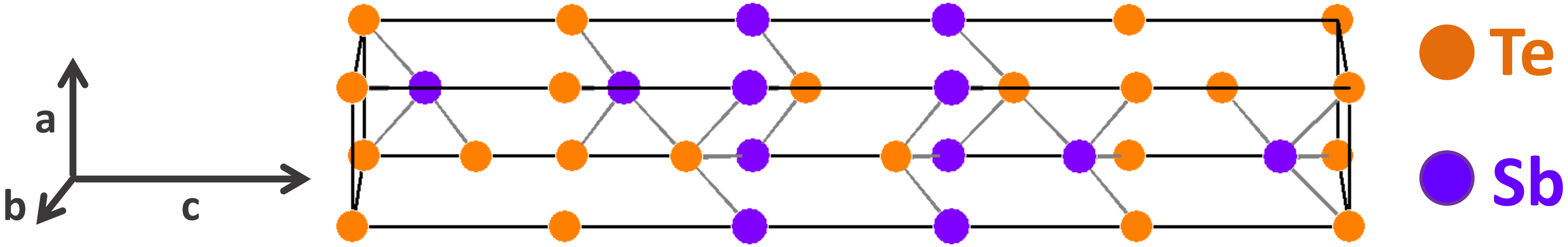
http://synapse.mdm.imm.cnr.it

Study of the **growth processes and functional properties** of **Ge- and In-based** NWs.

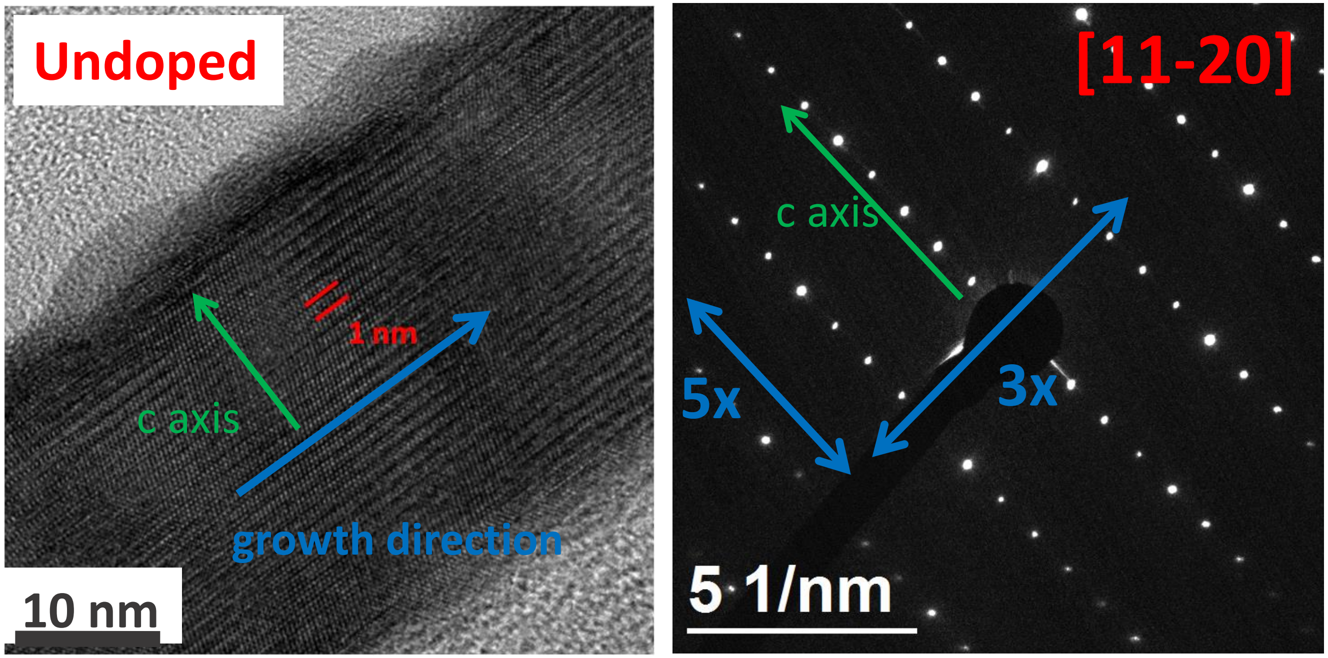
Investigation of the **phase change mechanisms** → Experimental work supported by **theoretical modeling and simulation**.

Realization of n**ew MOCVD-controlled chalcogenide NWs** with **optimized conditions**, → contribution to **improve the performances of next generation PCMs**.

Sb_2Te_3 Nanowires in their stable phase

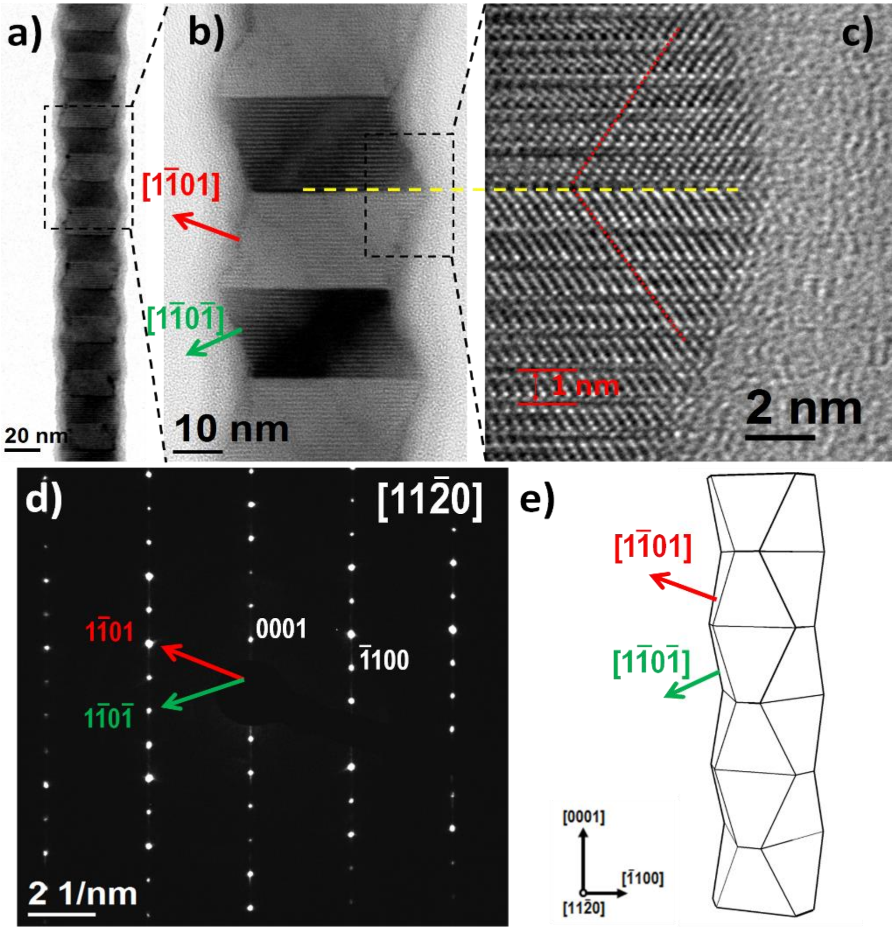


Space group **R-3m (#166)**, with lattice parameters a = 0.424 nm and **c = 3.0458 nm**
Stacking of **15 atomic planes**.



Super periodicity in the DPs is due to the *h+k+l=3n* selection rule characteristic of the R-3m (#166) space group.

A novel Sb_2Te_3 polymorph by MOCVD-VLS

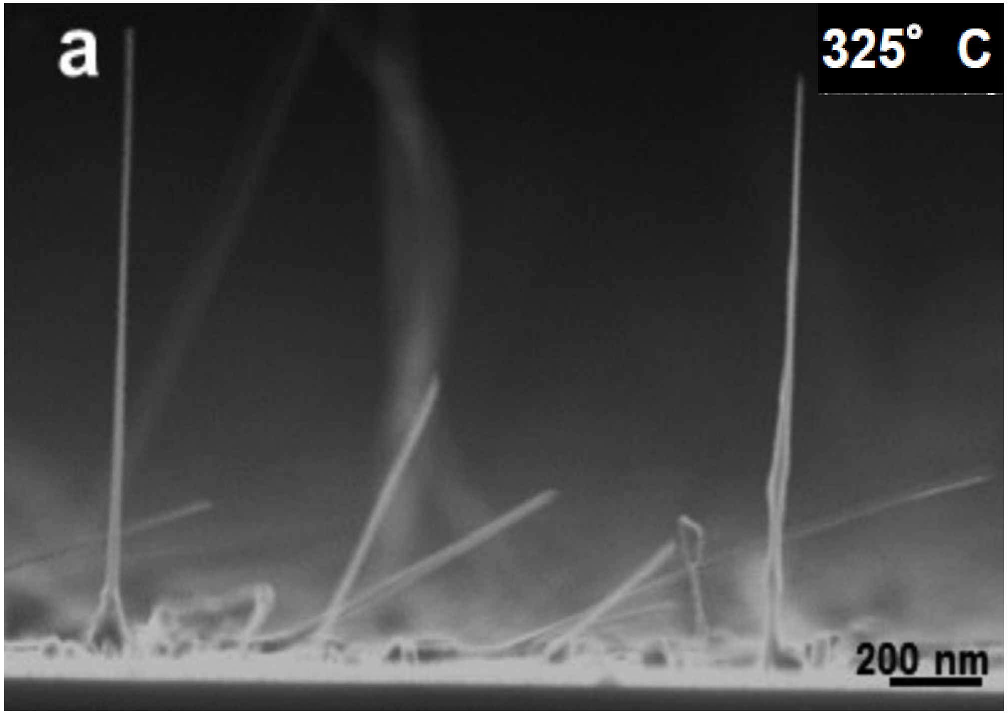


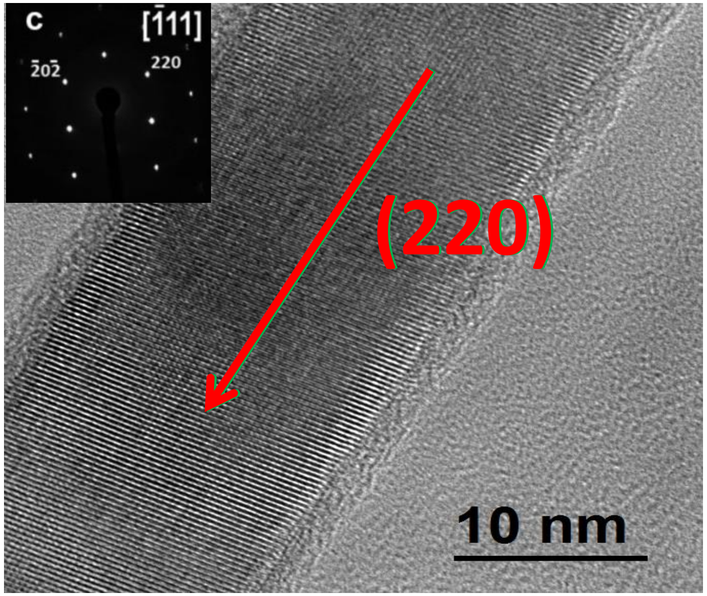
No selection rule observed in the diffraction pattern. The structure of the metastable NW is not compatible with the R-3m (SG#166) space group.

The NWs having diameter smaller than 40 nm present a very regular array of defects (twin planes) along the whole NW length.
The defects give the NWs a zig-zag shape.

E. Rotunno et al. Chem. Mater., 2015, 27 4368

NW synthesis on Si(001) at 300 mbar





15 nm < d < 30 nm
1 µm < L < 3 µm

EDX: $In_3Sb_{1.3}Te_{2.3}$
DP: $In_3Sb_1Te_2$ rock salt

NW with optimized morphological-structural properties for PCM

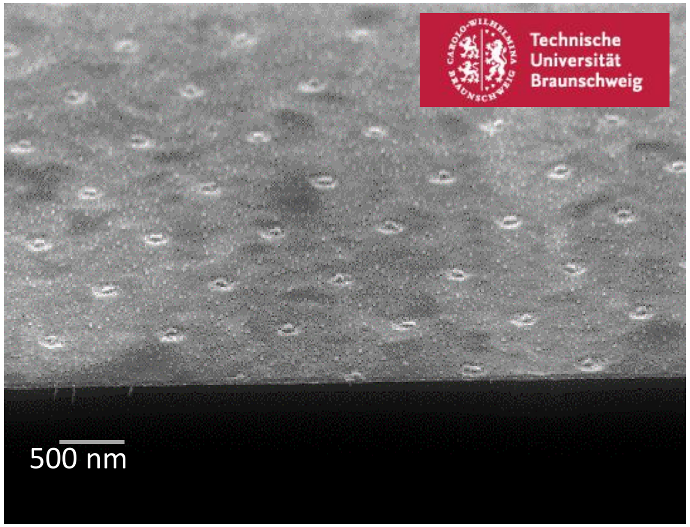
S. Selmo et al.
Phys. Status Solidi A (2016)

⇨ S. Selmo, poster *K:HP13*

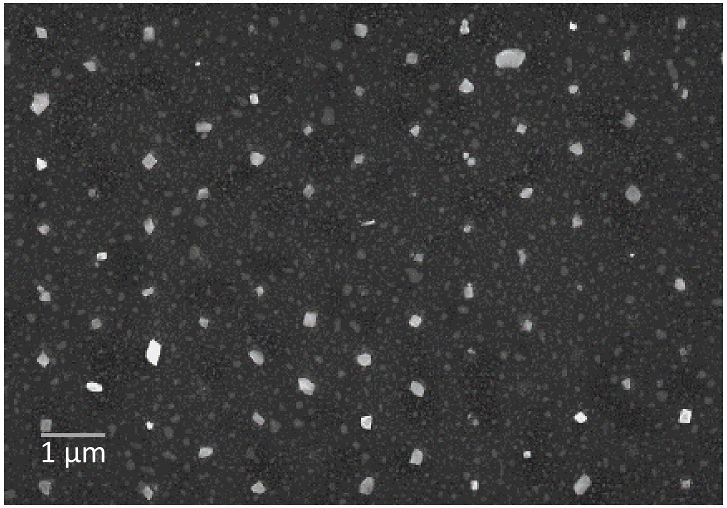
IST NW positioning on Nanoimprinted templates

Hole ϕ: 200 ÷ 300 nm and pitches ≈ 1 μm

Au film ≈ 5 nm and SiO_2 = 30 nm



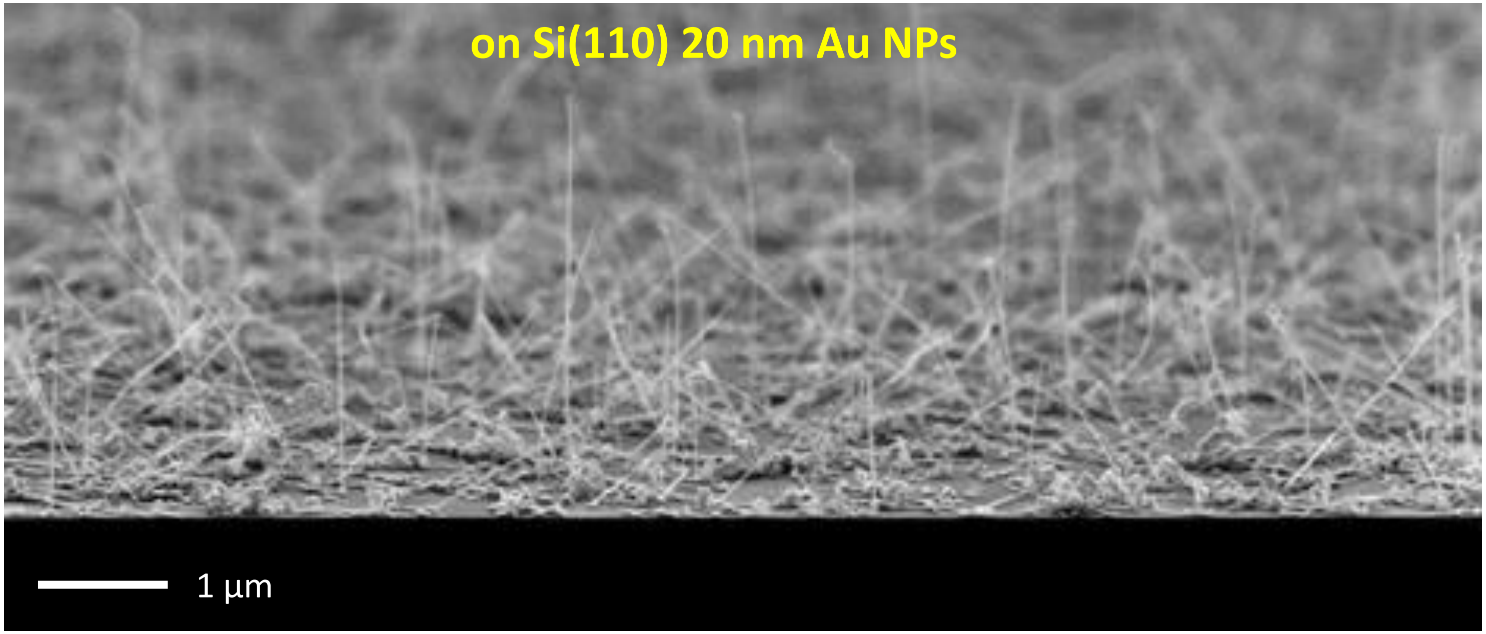
MOCVD



Selective growth but only crystals

- Crystal composition: $In_{50}Sb_{10}Te_{30}Ge_{10}$ (at %)
- unexpected presence of Ge

In-Ge-Te NWs oriented growth



Morphology and growth orientation

- High density
- Length: 1 – 3 µm
- Diameter: 15 - 50 nm (increasing with NPs size)
- High orientation; growth orientation || Si <110>

Size effects in phase change NWs

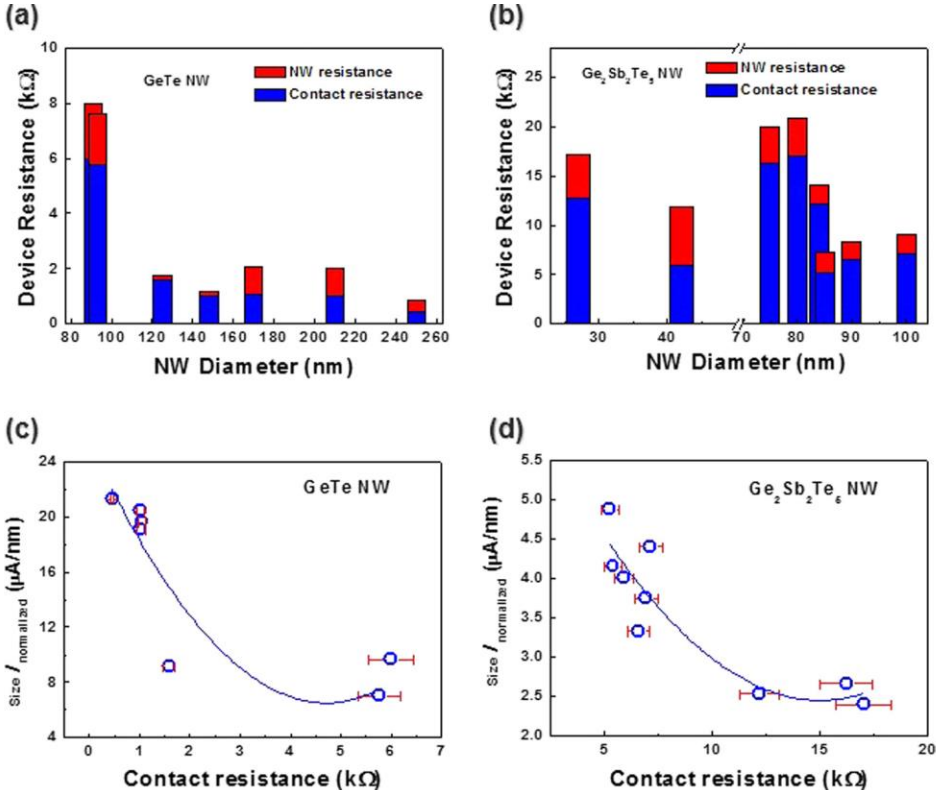
$$\frac{T_m(D)}{T_m(\infty)} = \exp\left(-\frac{2S_{vib}(\infty)}{3R}\frac{1}{(D/D_0-1)}\right)$$

D = NW diameter

Material	T_m bulk (°C)	T_m nanowire (°C)	Reference
GeTe	725	410 390	Lee *et al.* (2008) Sun *et al.* (2007)
In_2Se_3	890	680 722.5	Sun *et al.* (2006) Jin *et al.* (2013)
$Ge_2Sb_2Te_5$	616	375	Lee *et al.* (2008)
Ge	930	650	Wu and Yang (2001)

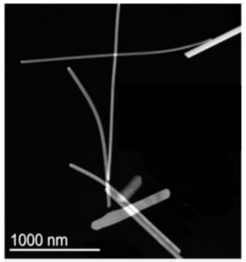
Melting temperature

M. Longo, Woodhead Publishing, 2014.



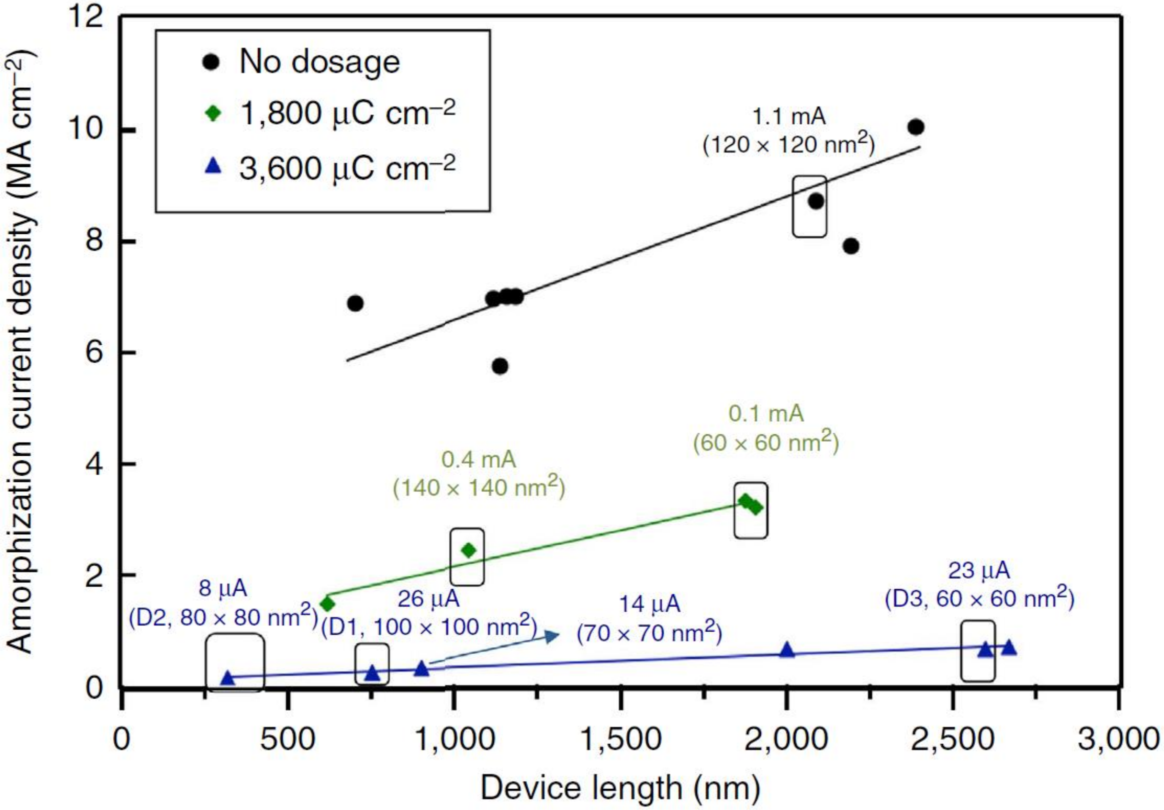
Contact resistance-reset current

Hwang et al. Appl. Phys. Lett. 106, 193106 (2015)



- **Melting temperature** ⬇
- **Crystallization temperature - retention** ⬇
- **Reset currents and power consumption** ⬇
- **Activation energy for re-crystallization** ⬇
- **Resistance drift** ⬇
- **Thermal conductivity** ⬇
- **Reduced thermal crosstalk** ⬇

Low power switching by NW defect engineering in GeTe NWs



Improvement in amorphization current densities achieved by carrier localization near the Fermi level (extended defects induced by 2MeV He^+ ion irradiation).

SiO_2 passivated GeTe NW devices amorphized via the defect-based pathway, at current densities of 0.13 – 0.5 $MAcm^2$ << 50 $MAcm^2$ of melt-quench pathway.

Nukala et al., NATURE COMMUNICATIONS, 7 (2016) 10482

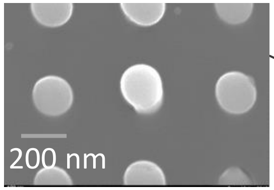
IGT NW arrays: UV lithography on $CoSi_2$ film

Templates with Metal

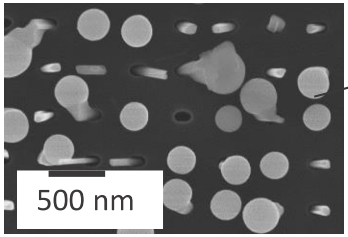
MOCVD on $CoSi_2$ film vs Au NPs
SAG vs VLS

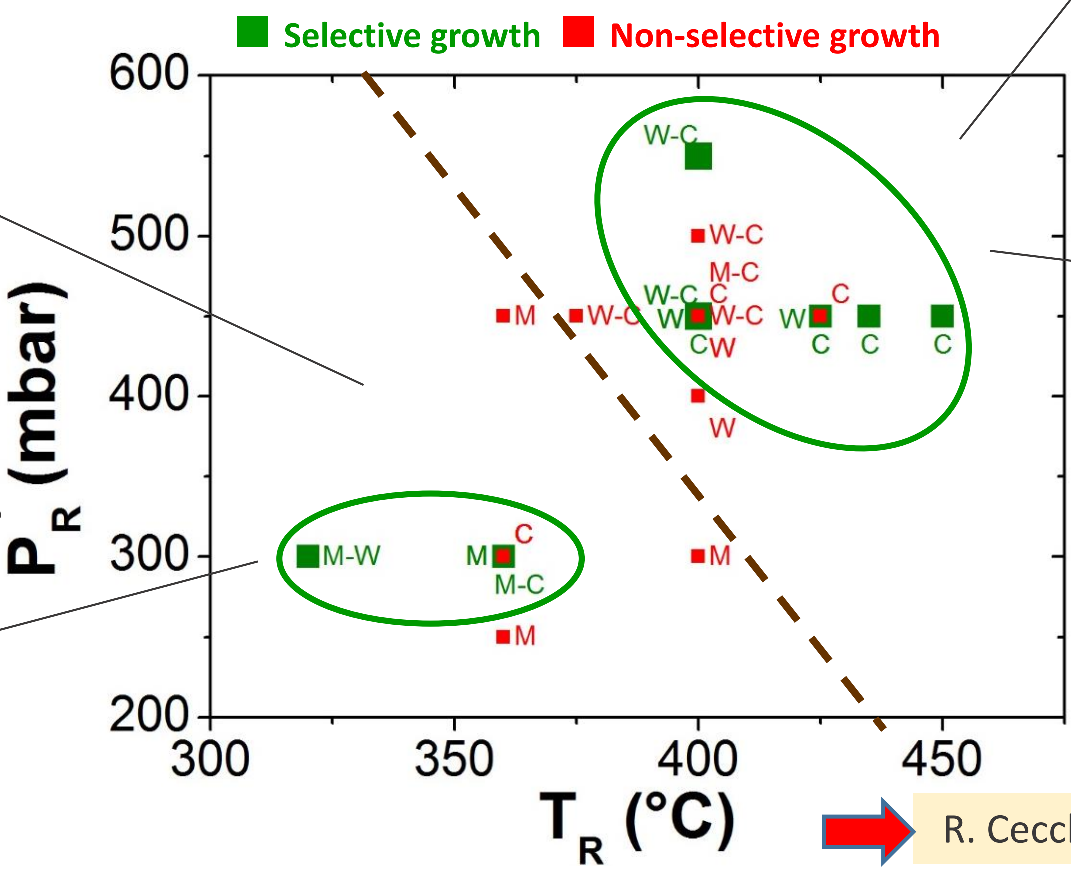
M = "Mushroom"-like
W = "Wire"-like
C = "Crystal"-like

"M" InTe

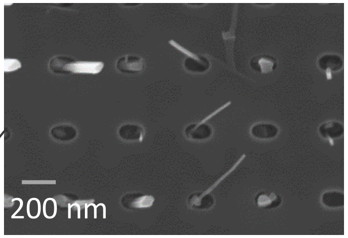


"M" & "W" InGeTe

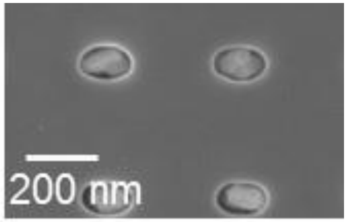




"W" InGeTe

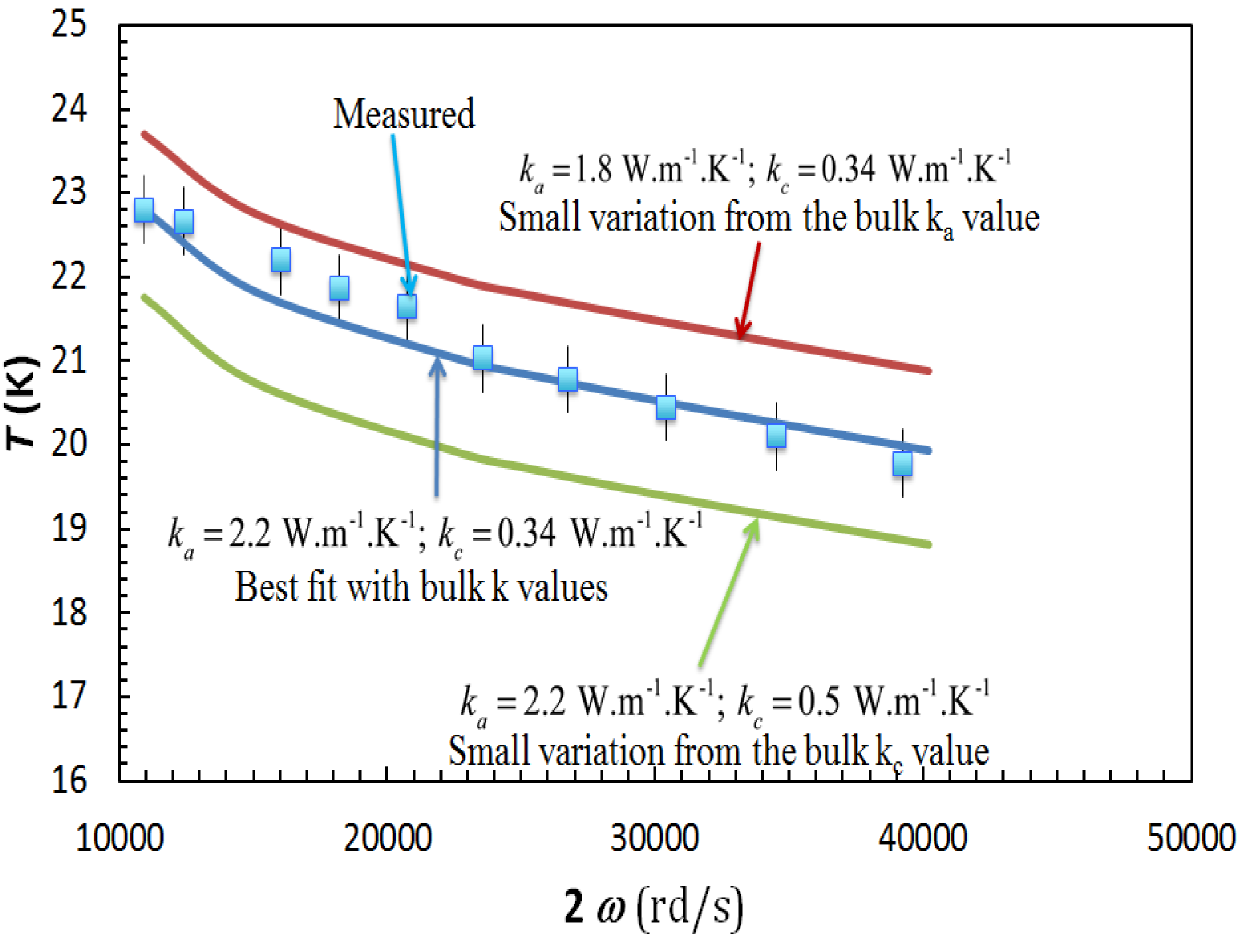


"C" InGeTe



R. Cecchini, presentation *K-2:L06*

Temperature rise of the heated Pd strip on the SThM probe



Very good agreement between the measured temperature and the calculated one by using the theoretical thermal bulk conductivity (k_c and k_a) for Sb_2Te_3 (the characteristic length for the film and the NW >> phonon mean free path).

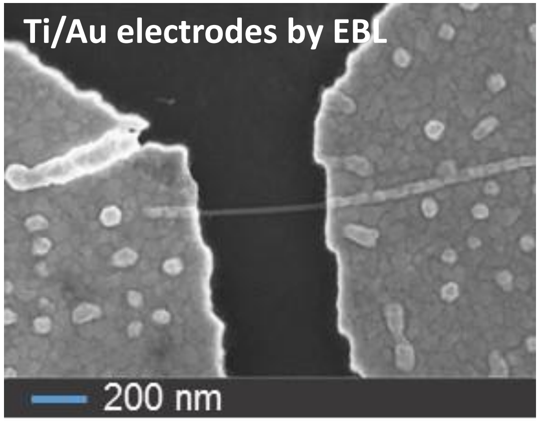
M. Longo, NANOFIM2015
ISBN: 9 788896 496381

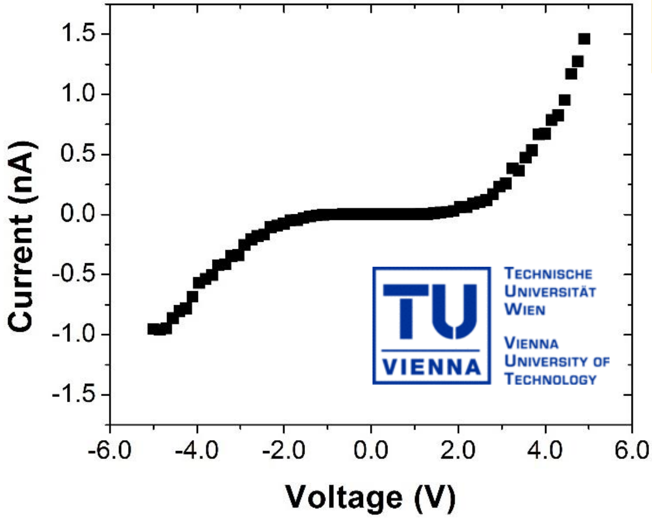
Electrical switch properties compared

	Material and NW diameter (D)	Switching cycles	Programming current	Threshold Voltage (V)
NWs	GeTe NW D=100 nm	NA	~0.5 mA for set - ~1.5 mA for reset	0.8
	GST NW D=60 nm	> 10^5	0.25 mA for set	1.8
	$Ge_1Sb_2Te_4$ NWs D= 80 nm	9	NA	1.35
	$Ge_{0.2}Sb_3Te_{6.8}$ NWs 50 nm	A few	NA	NA
	GST NW, in a nanogap aligned to CNT D=40 nm+SiO_2 passivation	>10^3	0.1 µA for set 1.6 µA for reset	3.2
	In_2Se_3 NWs D=100-350 nm+ SiO_2 passivation	> 20	NA	NA
	Sb_2Te_3 NWs D=99 nm	10	NA	0.75
	Bi_2Te_3 NW, array	≈ 50	NA	1.2
	Ge-Sb NWs D=70-100 nm	200	0.24 mA for set	4
	$In_3Sb_1Te_2$ NW, D=70 nm	NA	NA	1.6
Lytho	Sb_2Te line memory cell	10^7	280 µA	NA
	Doped Ge-Sb bridge cell	>10^4	60 µA for set - 90 µA for reset	~1
	GST NW by EBL – width 39 nm	NA	2µA for set	1.81
Confined	7.5 nm Dash-Type Confined PCM cell	$2x10^{10}$	160 µA for reset	0.65
	Lateral PCM/CNT	200	1 µA for set - 5 µA for reset	3.5
	GeTe Cross-point PCM with CNT electrodes	>100	1.4 µA for reset	5-13
	45 nm Microtrench GST PCM cell	>10^8	200 µA for reset	NA
	Cross spacer	>10^6	230 µA	NA
	Interfacial PCM	>10^7	~0.2 mA for set ~0.6 mA for reset	NA

M. Longo, Chapter 7, “Nanowire phase change memory (PCM) technology: properties and performance” in “Advances in Non-volatile Memory and Storage Technology”, Woodhead Publishing, Ed. Y. Nishi, 2014.

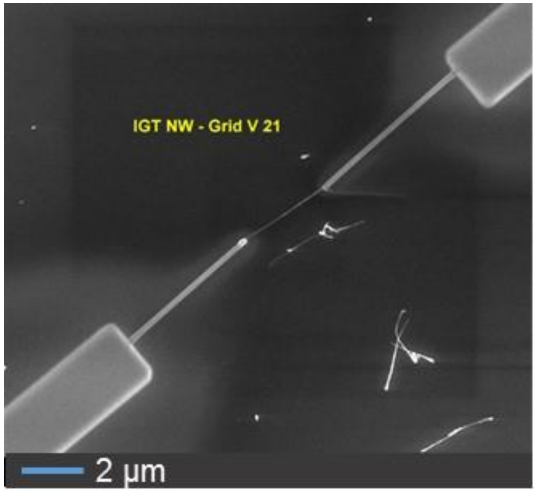
NWs preliminary electrical analysis

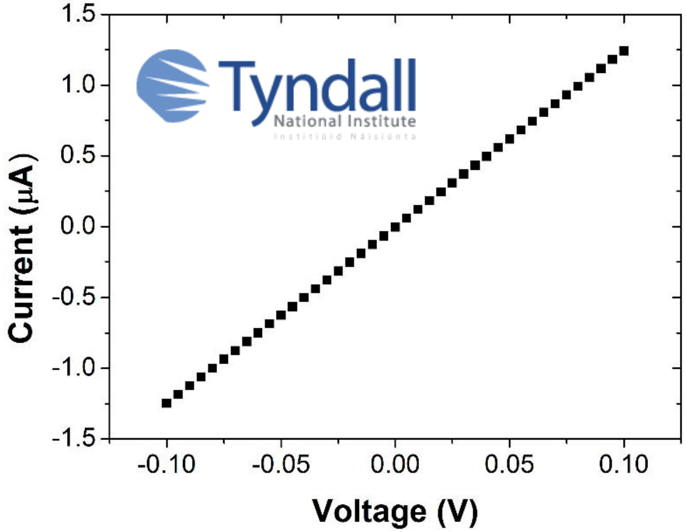




Core-shell Ge-InTe

- High resistance ≈ GΩ (contacts)
- Non-linear I-V
- Ge (core) dominated transport?





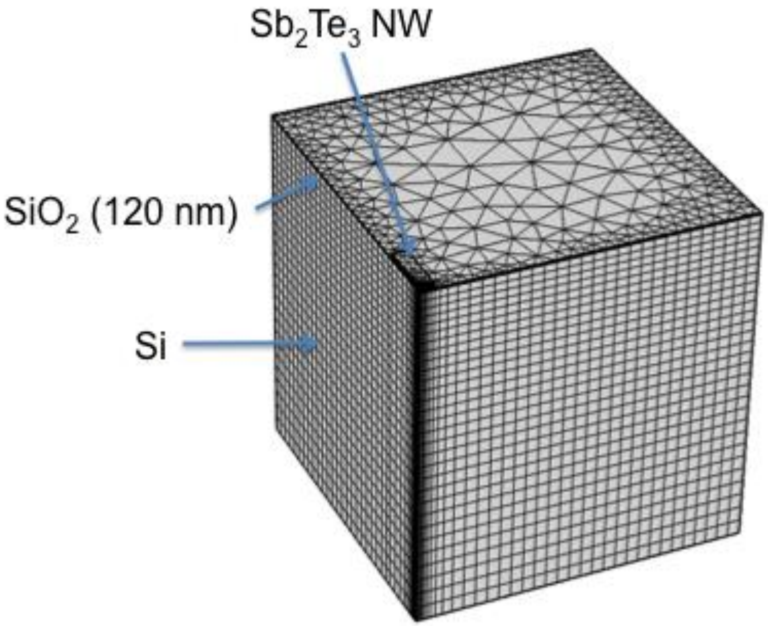
Ternary InGeTe

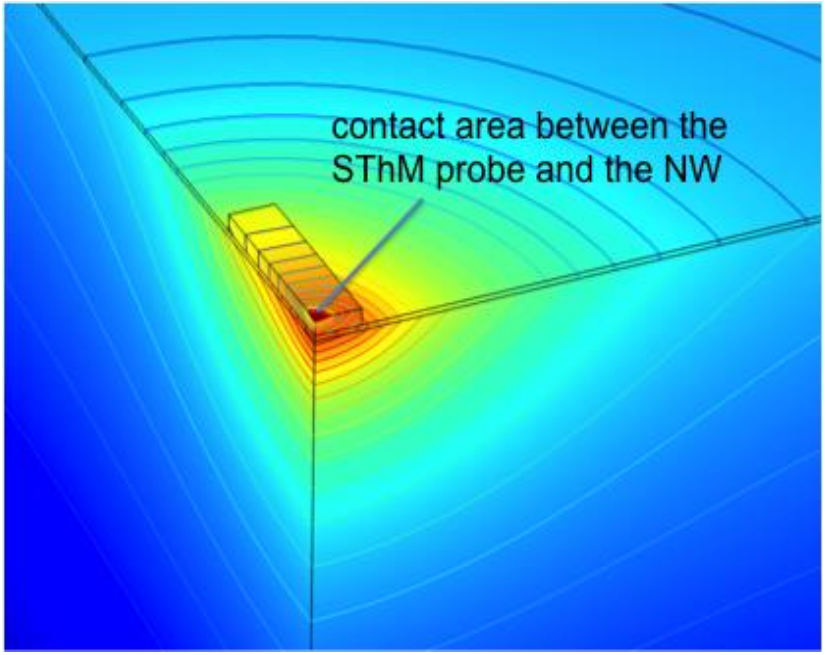
- Linear I-V
- Resistance OK
- $\rho_{NW} = 4\ m\Omega\cdot cm$ ($\approx \rho_{x\text{-}GST225}$)

(ready for pulsing…)

Heat transfer simulations in the Sb_2Te_3 NWs

- **c-axis perpendicular to the NW axis**
- **Low carrier density of 2.3×10^{18} cm^{-3}**





Heat transfer in the SThM experimental configuration is simulated using the finite element method.

Simulated temperature field (zoom centered on the NW) in the [NW+SiO_2+Si] system at 1200 Hz.

M. Longo, NANOFIM2015
ISBN: 9 788896 496381

The anisotropy on the NW is involved in the calculated average temperature of the heated area.